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METAMUTATOR:
ITS REALIZATIONS AND ITS APPLICATIONS

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METAMUTATOR: ITS REALIZATIONS AND ITS APPLICATIONS

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METAMUTATOR: ITS REALIZATIONS AND ITS APPLICATIONS

Abstract

Mutators became very popular after 1971, when Leon Chua realized the memristor, his postulated fourth circuit element, using them. The reason for the popularity of mutators, which are easily realizable 2-port devices, lies in the fact that they render possible the simulation/emulation of, hence experimentation with, postulated non-existing (not off the shelf available) elements like memstors.[1]

On the other hand, in the literature when simulating/emulating elements with 2-ports, many 4-port "generalized mutator-like" realizations that nobody has been able to identify are being used. These underlying 4-ports, and their ability to act as a mutator when two of the ports are properly terminated, have been thus named *metamutator*.

In this thesis, in addition to introducing some of metamutator realizations, newly designed metamutator circuits with one or two active devices are introduced. Also, a new active device, with only twelve transistors, named Additive and Differential IC (AD-IC), is proposed with its layout and use in metamutator circuit design. In addition, many 1-port and 2-port circuit realizations using metamutators have been introduced. 1-port applications are memstor simulation/emulation, floating and/or grounded impedance scaling which comprise inductance simulation, capacitance multiplication, oscillators and Frequency Dependent Negative Resistor (FDNR) simulation. 2- port applications cover Voltage Mode Multiple Input Single Output (VM-MISO) and Current Mode Single Input Multiple Output (CM-SIMO) universal filters and implementations of transconductance and transimpedance amplifiers. Also, two different applications of AD-IC: AD-IC based analog multiplier and AD-IC based full-wave rectifier are proposed in the thesis.

Keywords: Mutator, memstor, memristor, metamutator, universal filter, FDNR, analog multiplier, RC-oscillator, AD-IC

[1]Memstor is a generic name for memristor, memcapacitor, meminductor and memristance, meminductance, memcapacitance respectively.

METAMUTATOR: GERÇEKLEMELERİ VE UYGULAMALARI

Özet

Leon Chua'nın 1971 yılında memristorları, onları kullanarak gerçeklemesinden sonra mutatorlar ilgi odağı olmaya başladılar. Mutatorların ilgi çekmelerinin nedeni piyasada bulunmayan yeni ortaya atılmış memristor gibi, ya da bobin benzeri entegre devre teknolojisi ile uyumlu olmayan elemanların mutator devreleri kullanarak simüle/emüle edilebilmesidir.

Diğer yandan, literatürde 2-kapılılar ile elemanlar simüle/emüle edilirken, kişiler farkına varmadan çoğu zaman genelleştirilmiş mutator benzeri bir 4-kapılı yapı kullanmışlardır. Altta yatan bu gizli 4-kapılılar ve bunların iki kapıları uygun sonlandırıldığında diğer iki kapıdan mutator gibi davranmaları, metamutator adının takılmasına neden olmuştur.

Bu tezde metamutatorun, farkına varılmayan gerçeklenmeleri ve yeni geliştirilmiş bir veya iki aktif elemanlı devreleri verilmiş ve sadece on iki tranzistor kullanılarak yeni tasarlanmış bir toplayıcı ve çıkarıcı entegre devresi ile (AD-IC) bu devre tabanlı bir metamutator tanıtılmıştır.

Ayrıca metamutator kullanarak çeşitli 1-kapılı ve 2-kapılı gerçeklemeleri ile bunların birçok farklı uygulamaları tanıtılmıştır. 1 kapılı devre gerçeklemeleri ile yapılmış uygulamalara örnek olarak, endüktans simülatörü, kapasitans çarpım devresi, frekansa bağlı negatif direnç, osilatörler ve yüzer veya topraklanmış empedans dönüştürme uygulamaları tanıtılıp simülasyonları yapılmıştır. 2 kapılı olarak yapılmış uygulamalara örnek olarak: transkondüktans ve transempedans kuvvetlendiricileri, gerilim modlu çok girişli tek çıkışlı ve akım modlu tek girişli çok çıkışlı evrensel süzgeçlerin uygulamaları yapılmıştır. Ayrıca, bu tezde AD-IC tabanlı iki farklı uygulama da önerilmiştir. Birincisi AD-IC tabanlı analog çarpma devresi, ikincisi AD-IC tabanlı tam dalga doğrultucu devresidir.

Anahtar kelimeler:mutator; memstor; memristor; metamutator; evrensel filtre; FDNR; çarpma devresi; osilatör; AD-IC

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To

My husband Shahram

&

My parents Homa & Reza

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List of Abbreviations

AC	**A**lternative **C**urrent
ADC	**A**nalog to **D**igital **C**onverter
AD-IC	**A**dditive- and **D**ifferentiative **I**ntegrated **C**ircuit
AM	**A**mplitude **M**odulator
Ap	**A**ll **P**ass
BP	**B**and **P**ass
CCCDBA	**C**urrent **C**ontrolled **C**urrent **D**ifferencing **B**uffered**A**mplifiers
CCCII	**C**urrent **C**ontrolled **C**urrent **C**onveyor
CCII+	**P**lus **T**ype **II.** generation **C**urrent **C**onveyor
CCII-	**M**inus **T**ype **II.** generation **C**urrent **C**onveyor
CF	**C**urrent**F**ollower
CFOA	**C**urrent **F** eedback **O** perational **A**mplifier
CIM	**C**urrent**I**nverting **M**etamutator
CM	**C**urrent**M**ode
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
DC	**D**irect **C**urrent
DOCCII	**D**ual **O**utput **C**urrent **C**onveyor
DO-OTA	**D**ual **O**utput **O**perational **T**ransconductance **A**mplifier
DSBSC	**D**ouble **S**ideband **S**uppressed **C**arrier **A**lternative **C**urrent
DVCC	**D**ifferential **V**oltage **C**urrent **C**onveyor
DXCCII	**D**ual**X** **C**urrent **C**onveyor
FDCCII	**F**ully **D**ifferential **C**urrent **C**onveyor
FDNR	**F**requency **D**ependent **N**egative **R**esistor
HP	**H**ewllet **P**ackard

HP	**H**igh **P**ass
JFET	**J**unction **F**ield **E**ffect **T**ransistor
KCL	**K**irchoff's **C**urrent **L**aw
KVL	**K**irchoff's **V**oltage **L**aw
LP	**L**ow **P**ass
MC	**M**em**C**apacitor
ML	**M**em**I**nductor
MR	**M**em**R**istor
NMOS	**N**egative **M**etal **O**xide **S**emiconductor
OPAMP	**OP**erational **AMP**lifier
OTA	**O**perational **T**ransconductance **A**mplifier
PMOS	**P**ositive **M**etal **O**xide **S**emiconductor
TSMC	**T**aiwan **S**emiconductor **M**anufacturing **C**orporation
VIM	**V**oltage **I**nverting **M**etamutator
VM	**V**oltage **M**ode

Chapter 1

Introduction

1.1 Basic Circuit Elements and Memstors

As it is well known there are four basic circuit variables: electrical charge q, current i (being the derivative of charge), voltage v and flux φ (being the derivative of flux); also only three fundamental, two-terminal circuit elements were known and used: resistor, capacitor and inductor. The behavior of these circuit elements is described by an algebraic relationship between two of the four basic circuit variables.

$f_R(i, v) = 0$	Resistor
$f_C(q, v) = 0$	Capacitor
$f_L(\varphi, i) = 0$	Inductor

TABLE 1.1: Basic circuit elements.

According to Table 1.1 a symbolic graph can be visualized that depicts the constitutive (defining) relations between current-voltage, charge-voltage and flux-current respectively as shown in Figure 1.1. It is the missing link between flux φ and electrical charge q that led to the discovery of memristor.

In 1971, Leon Chua completed the symmetry by introducing the relation between φ and q and, calling the resulting element a memristor an acronym obtained by combining MEMory and ResISTOR. Thus a memristor is a 2-terminal circuit element with an algebraic constitutive relation between its charge and flux [1].

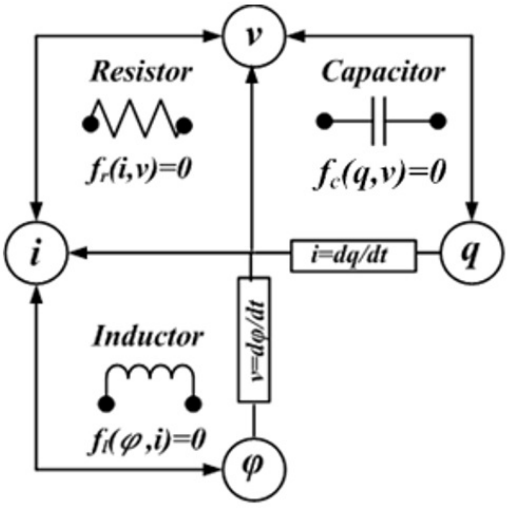


Figure 1.1: Basic circuit variables and fundamental 2-terminal elements

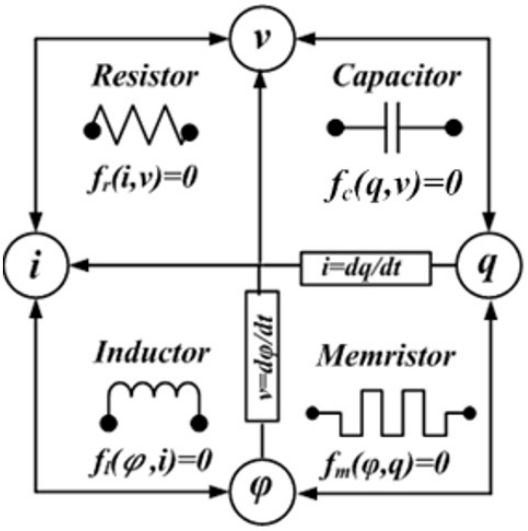


Figure 1.2: The fourth element memristor completing the symmetry [1]

The general expression of a time-invariant memristor is:

$$f_M(\varphi, q) = 0 \tag{1.1}$$

The symbol and a hypothetical φ-q curve of the memristor are shown in Figure 1.3.

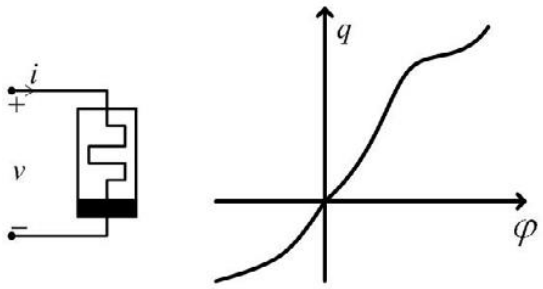


Figure 1.3: Symbol of memristor and its φ-q characteristic

Based on dependency between charge and flux of memristor there are two types of memristors: charge controlled and flux controlled memristors.

If φ is a function of q the memristor is *charge controlled*, if q is a function of φ the memristor is *flux controlled*. For a charge controlled memristor:

$$\varphi = f(q) \tag{1.2}$$

Assuming that f in (1.2) is differentiable, by taking time derivative of both sides of (1.2) and applying the chain rule the v-i dependence for a memristor becomes:

$$v(t) = \frac{d\varphi(t)}{dt} = \frac{df(q)}{dq}.\frac{dq}{dt} = M(q(t)).i(t) \tag{1.3}$$

Thus,

$$v(t) = M(q(t)).i(t) \tag{1.4}$$

where $M(q(t)) = df(q)/dq$ is the Memristance with Ohm (Ω) as unit, justifying the inclusion of "ristor" into the name.

In a *flux controlled* memristor the charge q is a function of φ,

$$q = f(\varphi) \tag{1.5}$$

Again by taking time derivative of both sides of (1.5) and applying the chain rule, (1.6) becomes:

$$i(t) = \frac{dq(t)}{dt} = \frac{df(\varphi)}{d\varphi}.\frac{d\varphi}{dt} = W(\varphi(t)).v(t) \tag{1.6}$$

Thus,

$$i(t) = W(\varphi(t)).v(t) \tag{1.7}$$

where $W(q(t)) = df(\varphi)/d\varphi$ is Memductance and has the unit of Siemens ($\mho$).

Comparing (1.4) and (1.7), one obtains:

$$M(q(t)) = \frac{1}{W(\varphi(t))} \tag{1.8}$$

Again from (1.4) and (1.7) it is easily observed that when the current through the memristor is zero its voltage is also zero, and vice versa thus forcing the characteristic to go through the origin. Thus by applying a sinusoidal current or voltage signal to the memristor its current-voltage characteristic becomes a Lissajous curve also passing through the origin.

In 1976, Chua and Kang in [2] introduced memristive systems by extending the concept of memristor to a class of nonlinear dynamical systems and in 2010 Ventra et al. extended the notion of memristive systems to capacitive and inductive elements with properties depending on the state and history of the system just like memristor [3]. By applying sinusoidal inputs all these elements show pinched hysteretic loops between two constitutive variables that define them: *current-voltage* for memristor, *charge-voltage* for memcapacitor, and *current-flux* for meminductor.

Finally, it should be observed that for a linear memristor $M(q)$ and $W(\varphi)$ reduce to constants hence to simple linear resistors, explaining why memristor was discovered so late.

Memstor, a term introduced in [4], is a generic name for the class of 2-terminal elements with memory such as memristor, meminductor, memcapacitor, which are devices whose terminal behavior depends nonlinearly on the initial state and the history of the applied input to the system. All memstors are summarized in Table 1.2 where σ is the time integral of charge and ρ is the time integral of flux.

Charge-controlled memristor	$v(t) = M\left(q_0 + \int_0^t i(\tau)d\tau\right) i(t)$
Flux-controlled memristor	$i(t) = W\left(\varphi_0 + \int_0^t v(\tau)d\tau\right) v(t)$
Charge-controlled memcapacitor	$v(t) = D_M\left(\sigma_0 + \int_0^t q(\tau)d\tau\right) q(t)$
Flux-controlled memcapacitor	$q(t) = C_M\left(\varphi_0 + \int_0^t v(\tau)d\tau\right) v(t)$
Charge-controlled meminductor	$\varphi(t) = L_M\left(q_0 + \int_0^t i(\tau)d\tau\right) i(t)$
Flux-controlled meminductor	$i(t) = \Gamma_M\left(\rho_0 + \int_0^t \varphi(\tau)d\tau\right) \varphi(t)$

TABLE 1.2: Constitutive relations of all memstors

1.2 Literature Review

In 1968 Leon Chua in [5] claimed that it is possible to mutate one type of circuit element, be it linear or nonlinear, into another by using a 2-port mutator and he first proposed three types of mutators for this purpose. Then in 1971, after introducing "memristor" as the fourth circuit element, he presented the first M-R mutator circuit with a highly complex structure for the purpose of realizing memristors from nonlinear resistors [1].

Due to the invaluable properties of memristor such as non-volatile memory element and/or its nonlinear characteristics, this element has been used in various applications like the design of analog and digital circuits, neuromorphic circuits, chaotic systems etc. [6], [84], [85], [86], [87].

Hewlett Packard (HP) research team in 2008 successfully realized the first memristor as a simple 2-terminal device using thin film Titanium dioxide (TiO2), which can be viewed as a 2-terminal resistor with changing resistance depending on the voltage or current applied to it [83]. Despite this successful realization, memristors are not yet commercially available and their modeling is essential to memristor based circuit and system design. Thus researchers have been encouraged to develop simple SPICE macro models [120-124].

Another approach is the use of mutator circuits, constructed using off-the-shelf devices which are commercially available in the market [98-102], [104-105], [107], [109-112] to mutate the dynamic behavior of conventional elements to that of a memristor hence the need and emphasis on "Mutators". Mutators not only convert one type of element to another in simulations they also make hard realizations of unavailable 2-terminal elements possible and thus provide means to experiment in the lab with them.

A literature survey shows a very large number of mutator realizations, possessing weaknesses such as:

i. The use of an excessive number of active elements,

ii. Excessive use of grounded and/or floating passive elements,

iii. Usage of ungrounded capacitors; using grounded capacitors in integrated circuit (IC) implementation has considerable advantages [116],

iv. Use of analog multiplier for the purpose of obtaining nonlinearity property of memristor, causes to increasing the number of used active elements , which resulting in higher power consumption also large chip area occupation.

For instance, the memristor emulator presented in [113] uses a Microcontroller, an Analog to Digital Converter (ADC) and a Digital to Analog Converter (DAC) blocks and one low pass filter. This emulator is topologically complex which limits its applicability due to difficulty in interconnecting with active and passive devices. The proposed emulator circuit suffers from weakness i.

An Electronically Tunable Differential Different Current Conveyor (EDDCC) and a multiplier are used to implement the memristor emulator circuit proposed in [114]. Six OTAs are employed in the structure of EDDCC. However, the experimental results using this mutator circuit do not satisfy the properties of a memristor and the hysteresis loop area does not decrease as frequency increases. Also, the proposed emulator circuit suffers from weaknesses i and iv.

A CMOS based memristor emulator has been introduced in [115]. Single CCII+, one grounded capacitor and one Voltage Controlled Resistor (VCR) are employed in the implementation of the emulator. Also, two OPAMPs, a single transistor, two floating capacitors and six resistors are utilized in VCR implementation. Due to complexity of the structure and use of floating capacitors this emulator configuration is not suitable for real world hardware applications. Briefly the proposed emulator circuit suffers from disadvantages i, ii and iii.

In [98] a floating memristor with four OPAMPs, single analog multiplier, ten transistors, single capacitor and eight resistors in its structure was presented.

Both simulation and experimental results are given in the paper. There are three important properties to be considered in a memristor emulator: memory effect, frequency dependent characteristic, and nonlinearity. Memory effect and frequency dependency characteristic are obtained by using a capacitor. Nonlinearity is implemented using multiplier circuit. But each used block gives rise to extra power dissipation and more complex circuit also, simulations have not been performed at transistor level. Briefly proposed mutator circuit suffers from i, iii and iv.

Yesil et al. proposed a floating memristor emulator employing a single Differential Difference Current Conveyor (DDCC), one analog multiplier and two resistors, one floating and one grounded capacitor [99]. The capacitor provides the memory effect and the multiplication of capacitor and resistor voltages is connected to the Y terminal of the active device. However, the memristor can be operated only at high frequencies such as in the order of MHz which contradicts the essential properties of memristor also, the proposed mutator circuit suffers from weakness i.

In [100] a floating memristor emulator including four CFOAs, one multiplier and six passive elements in its structure have been proposed. Both simulation and experimental results are given in the paper. However, the simulations are not done at transistor level and the proposed memristor mutator circuit suffers from i, ii, iv.

In [101] a floating memristor emulator containing four CFOAs, single analog multiplier, single OPAMP and nine passive elements, where some of the elements are floating is presented. The memristance value of obtained memristor is not electronically tunable. The emulator circuit is complex, bulky, suffering from i, ii, iv.

In [104], a grounded memristor emulator made of two CFOAs, a single analog multiplier and seven grounded/floating passive elements has been proposed. The

optimal frequency range of the obtained memristor is 16Hz - 160kHz. Both simulation and experimental results of the presented memristor emulator have been given to confirm its feasibility and workableness. However, the simulations are not at transistor level and commercially available active devices have been used instead of CFOAs and analog multiplier. The proposed memristor mutator circuit suffers from weakness i, ii and iv.

A CCII based charge controlled memristor emulator containing single CCII, single analog multiplier, single floating resistor and a grounded capacitor was presented in [105]. However, the memristance value of obtained memristor is not electronically tunable. Also, commercially available active devices AD633 and AD844 have been utilized instead of multiplier and CCII+, respectively. Briefly the proposed emulator circuit suffers from disadvantages i, ii and iv.

A tunable floating memristor emulator circuit consisting of single multiple-output OTA (MO-OTA), single analog multiplier and two grounded passive elements was proposed in [106]. This emulator derived from the one in [99] has the advantage of its memristance value being adjustable by biasing the current of the OTA. The proposed emulator, despite its simplicity in design, suffers from iv.

One grounded voltage controlled and one grounded current controlled memristor emulators were reported in [107]. In the structure of current-controlled memristor emulator, two CCII+s, a single analog multiplier, a single buffer as active devices and three grounded one floating passive components are being used, while the voltage controlled memristor emulator consists of three CCII+s, a single analog multiplier, single buffer and six grounded passive elements. The circuit structures of both mutators are highly complex and suffer from weakness i, ii and iv. Also, the memristance values of obtained memristors are not electronically tunable.

Using single Current Backward Transconductance Amplifier (CBTA), single analog multiplier, two resistors and one grounded capacitor, a grounded memristor emulator is proposed in [108]. In this emulator Memory effect and frequency dependency properties of memristor are implemented by using a capacitor and

the nonlinearity property is obtained by using multiplier. The proposed emulator suffers from iv.

In [3] Pershin and Ventra, using off-the-shelf components like one microcontroller, one Analog to Digital Converter (ADC) and one digital potentiometer with its resistance defined by a digital code written in it, built a rather complex and expensive floating memristor emulator. The proposed memristor emulator suffers from i and ii.

In [102], a new floating memristor emulator consisting of three OTAs, four CCIIs, and seven passive elements, three of them floating, has been presented. Both simulation and experimental results of the presented memristor emulator have been given to confirm its feasibility and workability. Commercially available active devices CA3080 and AD844 have been used instead of OTA and CCII in simulations and experiments. However, the circuit configuration is complex and bulky and suffers from weaknesses i and ii.

In [103] a floating memristor emulator has been presented. The circuit of the emulator consists of one OTA, one multiplier, two MOS transistor and two grounded capacitors. The memristance value cannot be tuned electronically. The proposed emulator circuit suffers from iv.

A grounded memristor emulator employing ten DDCC active elements, eight transistors and five passive elements has been presented in [109]. However, the proposed emulator circuit suffers from i and ii. Each active device giving rise to extra power dissipation and a more complex circuit.

A generalized mutator for the purpose of realizing inductors, memristors, meminductors and memcapacitor has been reported in [4]. The memristor can be obtained by employing single adder, single subtractor, grounded diode, floating inductor and capacitor, without using an analog multiplier. The diode provides the non-linear resistor in the circuit. This circuit is able to convert all types of

circuit elements to each other and the idea of metamutator was first introduced in this article.

Two grounded memristor emulator configurations were presented in [110]. Each circuit comprises three CFOAs, four resistors, two capacitors, and one diode without using an analog multiplier. Nonlinear characteristic is provided by a diode. CFOA which is an active element, is modeled by AD844, a commercially available active device, and experimental results have been provided. Likewise, in [111], comprising of two CFOAs, a single OTA and five grounded passive elements a grounded memristor emulator again without using an analog multiplier is introduced. The proposed emulator circuits suffer from i and ii.

In [112] a grounded memristor emulator including Single Differential Voltage Current Conveyor Transconductance Amplifier (DVCCTA), one grounded capacitor, three resistors, one of them floating, is presented. Both simulation and experimental results of the memristor emulator are given in the paper. As for experiments a single CA3080, four AD844s and nine passive elements provided the implementation of DVCCTA. Due to its highly complex structure this emulator is not suitable for IC designs. The proposed emulator circuit suffers from i and ii.

In [119] a memristor emulator based on a light dependent resistor (LDR), with its resistance easily reconfigurable by a controlling voltage, is introduced. However, the memristance value of the memristor, realized due to the nonlinearity of the LDR, is hard to calculate accurately. Also the complexity and difficulty of practical implementation of the introduced emulator are the other disadvantages. The proposed emulator circuit suffers from i. ii and iii.

Memcapacitive and meminductive systems are two classes of circuit elements with memory that complete memstors ie. the class of memristive systems [1,2]. When driven by a periodic input, their characteristics are hysteretic loops between their constitutive variables current–flux for meminductors and voltage–charge for memcapacitors which pass through the origin [118]. Meminductor and memcapacitor are able to store energy and this significant ability distinguishes these elements

from memristor. Due to lack of availability of meminductor and memcapacitor as off the shelf components, just like the memristor, there are many different emulator circuits in literature for simulating meminductor and memcapacitor with active and passive components together.

In 2010 Pershin and Ventra, by using one OpAmp and several passive components, introduced mutator circuits for realizing lossy meminductors and lossy memcapacitors from memristors [7]. In simulations they have used the memristor emulator circuit in [3] and shown an interesting connection between three memory elements. The proposed emulator circuit suffers from iii.

In [8] a mutator circuit for mutating memristor to memcapacitor by employing inexpensive off-the-shelf components like, two OTAs and several passive components was reported. The presented mutator provides a true memristor into memcapacitor mutation. However, the proposed mutator is able to mutate only memcapacitor from memristor Also, simulations are not in transistor levels and for OTAs AD844 commercial device is used. In [9] mutator circuit for mutating memristor to memcapacitor is presented. The main idea of circuit design is the same as [8] and instead of two OTAs one CCII+ and one OTA is used in the structure of mutator circuit. In simulations the constitutive relation of the memristor is preserved, within scaling, by the elements obtained after the mutation Also simulation results confirm an important fingerprint of mem-elements, namely the gradually decreasing hysteretic effects with increasing input frequency. However, gain simulations have not been done at transistor level and AD844 commercial device is used instead.

In [11] different current conveyor based mutator implementations for converting memristor to both meminductor and memcapacitor have been proposed. Some of the implementations use a floating memristor. However only theoretical analyses are presented. Also, it is difficult to carry out these meminductor and memcapacitor mutators in practice since a reliable floating memristor emulator is necessarily required. Also the proposed circuits suffer from ii.

In 2014 Liang et al. presented a practical floating memristorless meminductor emulator circuit, using simple and inexpensive off-the-shelf components like four CCII+s, two operational OPAMPs, single analog multiplier, and several passive components in [16]. The proposed mutator circuit suffers from all of drawbacks mentioned above (i,ii,iii and iv). Also in simulations commercially available active devices CA3080 and AD844 have been utilized instead of CMOS based OTA and CCII, respectively and simulations have not been done at transistor levels.

It is very important to observe that all of the above mutator simulators/emulators can only serve one purpose namely, that of behaving like a 2-port mutator for mutating one circuit element to a memstor. The 4-port metamutator used in this thesis, besides behaving like a mutator, is a multi-purpose device that can be used in realizing/simulating/emulating many electronic devices such as Universal Filters, Transconductance/Transimpedance Amplifiers, Oscillators, Rectifiers and many more.

1.3 Generalized 4-Port Mutators: Metamutators

The first hard-realization shown in Figure 1.4 of memristor using a highly complex mutator circuit was introduced in [1]. Since then different types of much simpler mutator circuits have been proposed for realizing memristors using nonlinear resistors or memstors from memristor which were briefly described in Section 1.2.

The idea of a multi-functional 4-port mutator was first introduced in [4], then under the name of "Generalized Mutative 4-port" in [25] and then named as "Metamutator" because of its ability to implement a variety of elements/systems like memstors*, mutators, trans-admittance/trans-impedance amplifiers, multi-functional universal filters, quadrature oscillators, inverters, gyrators, multipliers etc. when some of its ports are properly terminated. Several IC designs of metamutators have been proposed and discussed in [12-14] and [24-26].

The general schematic block diagram of a metamutator is shown in Figure 1.4.

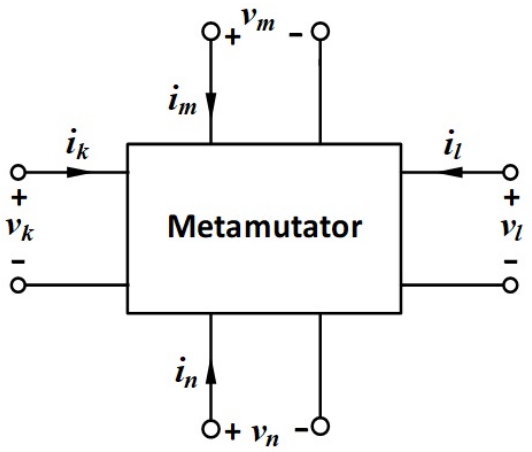


Figure 1.4: Block diagram of metamutator

According to the minus sign in the voltage or current in one of the ports, the class of metamutators can be separated into two sub-classes:

1. Voltage Inverting Metamutators (VIM)
2. Current Inverting Metamutators (CIM)

The 4-port block diagrams of VIM and CIM are shown in Figure 1.5 and Figure 1.6 and their mathematical port descriptions are defined via the equalities (1.9) and (1.10) respectively. Although identity matrices show in both expressions in VIM a port voltage is being inverted whereas, in CIM a port current is being inverted.

$$\begin{bmatrix} i_k \\ i_l \\ v_m \\ v_n \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_m \\ i_n \\ v_l \\ -v_k \end{bmatrix} \tag{1.9}$$

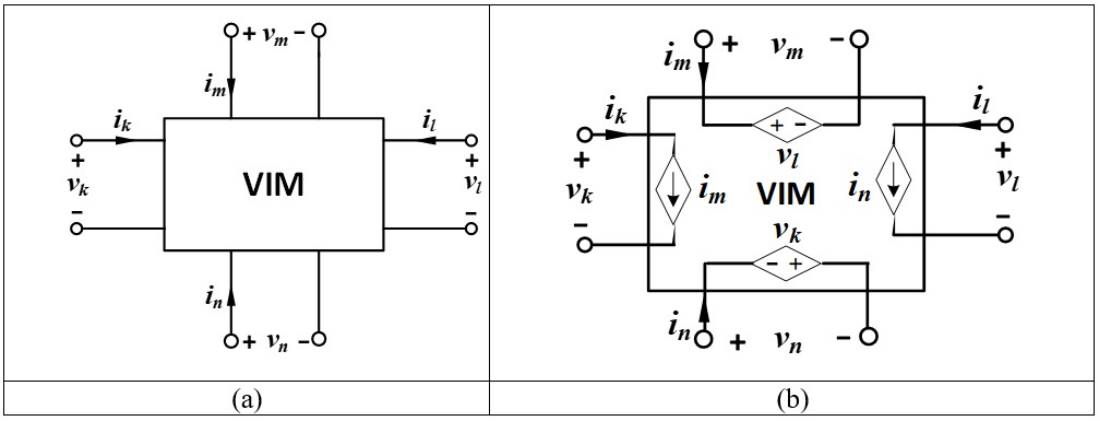


Figure 1.5: (a) Block diagram, (b) Circuit level realization of VIM 4-port meta-mutator

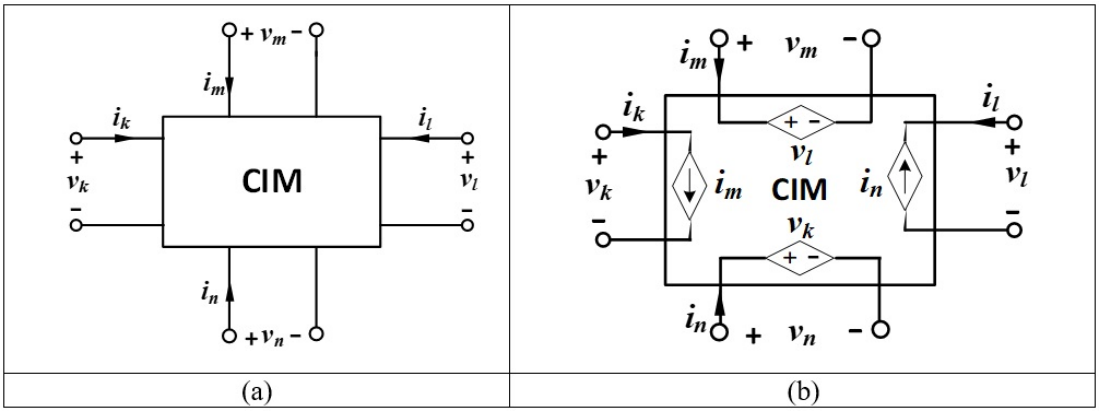


Figure 1.6: (a) Block diagram, (b) Circuit level realization of CIM 4-port meta-mutator

$$\begin{bmatrix} i_k \\ i_l \\ v_m \\ v_n \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_m \\ -i_n \\ v_l \\ v_k \end{bmatrix} \tag{1.10}$$

In (1.9) and (1.10) attention should be paid to port voltages' and port currents' reference directions; due to the – sign for the voltage v_k in (1.9) and the – sign for the current i_n in (1.10). Care must be exercised in the implementation phase as to which variable follows the other in (1.9) and (1.10); variables have been indexed with letters k, l, m, n taking different values from the set {1,2,3,4}.

These metamutators all share the same port descriptions hence possess the common property of becoming a different X-Y type mutator depending on how two of the ports are terminated. This in turn makes possible, via so created mutators, of mutating classical circuit elements to memstors or memstors to memstors. All of these terminations and mutations are listed in Table 1.3.

#	**Port** k	**Port** m	**Port** l	**Port** n	**Output Port**	**Element**
1	Resistor	Capacitor	Memristor	-	n	Meminductor
2	Capacitor	Resistor	-	Memristor	l	Meminductor
3	Memristor	-	Resistor	Capacitor	m	Meminductor
4	-	Memristor	Capacitor	Resistor	k	Meminductor
5	Memristor	Inductor	Resistor	-	n	Memcapacitor
6	Inductor	Memristor	-	Resistor	l	Memcapacitor
7	Resistor	-	Memristor	Inductor	m	Memcapacitor
8	-	Resistor	Inductor	Memeristor	k	Memcapacitor
9	Capacitor	-	Inductor	NL Resistor	m	Memristor
10	NL Resistor	Inductor	-	Capacitor	l	Memristor
11	-	Capacitor	NL Resistor	Inductor	k	Memristor
12	Inductor	NL Resistor	Capacitor	-	n	Memristor

TABLE 1.3: Mutation table for realizing 1-port elements [4].

1.4 Thesis Outline

In the first chapter of this thesis a brief introduction to basic circuit elements together with a new class of memory elements namely, memstors have been presented. In the same chapter, the necessity of using mutators and previously developed mutator circuits in the literature have been studied. Also a brief introduction to 4-port metamutators, their classification, according to their port description matrices, into two categories, Voltage Inverting Metamutator (VIM) and Current Inverting Metamutator (CIM) have been presented.

In the second chapter the necessity of using mutators and the basic definition of 2-port mutators with their ports relation matrices and the mutators themselves

for mutating nonlinear circuit elements to memristors or converting memristors to other non-volatile circuit elements like meminductor and memcapacitor have been presented also some of the previously developed classical mutator circuits, well-known in the literature, have been investigated.

In the literature there are many incognito 4-port mutator structures embedded in electronic circuits such as simulators/emulators. Nobody has been able to identify these underlying 4-ports and their ability to act as a Metamutator. With the third chapter in addition to introducing some of these incognito metamutator realizations, newly designed metamutator circuits, with one or two active devices in their structures, have been presented. Also, a novel realization of metamutator with a new single active device, Additive and Differential IC (AD-IC) along with the implementation of AD-IC with twelve transistors, has been proposed.

In the fourth chapter, different applications of metamutators developed during the research period of this thesis have been presented. As the port description matrix of all introduced metamutators in Chapter 3 are the same, all of these applications stand true for all of metamutators. Depending on how some of the ports are terminated, metamutator applications, can be classified in two groups, as follows:

I. 1-port circuits realized with metamutators,

II. 2-port circuits realized with metamutators.

For example, in 1-port realizations, by properly terminating three ports of the metamutator the resulting circuit may behave as mutator, floating and/or grounded impedance scalor, RC- oscillator. On the other hand, in 2-port realizations, by properly terminating two ports of the metamutator the resulting circuit may behave like a transconductance amplifier, transimpedance amplifier, voltage or current mode multiple input single output universal filter and single input multiple output universal filter. All of these applications have been presented in

Section 4.2 and examined in detail with PSPICE simulations using transistor parameters obtained from layout level descriptions of metamutators; comparison of simulation and theoretical results have also been presented in the same section.

In the fifth chapter of this thesis a voltage multiplier with single AD-IC and two squarer circuits in its structure and a full-wave rectifier again with an AD-IC and two diodes in its configuration have been presented. Both of the circuits were simulated with parameters extracted from the layout and simulation results show very good conformity with desired voltage multiplier and full-wave rectifier behaviors. Also a comparison of the proposed analog multiplier and full-wave rectifier with others, existing in the literature, are included into this chapter.

Conclusions and future research directions conclude the thesis in the fifth chapter followed by a list of references and appendices containing PSPICE Netlists and other implementation programs.

Chapter 2

Mutator Circuits and Memstor Simulations

First in 1968 Leon Chua in [5] claimed that it is possible to mutate one type of circuit element, be it linear or nonlinear, into another by using a two-port mutator and he first proposed three types of mutators for mutating circuit elements to each other. In 1971, he also presented a new class of mutators, for mutating nonlinear circuit elements to memristors and vice versa [1]. According to [1] there are several types of circuit realizing the same kind of mutators which mutate element type X into element type Y, called X-Y mutator. The symbolic 2-port structures of these mutators are shown in Figure 2.1.

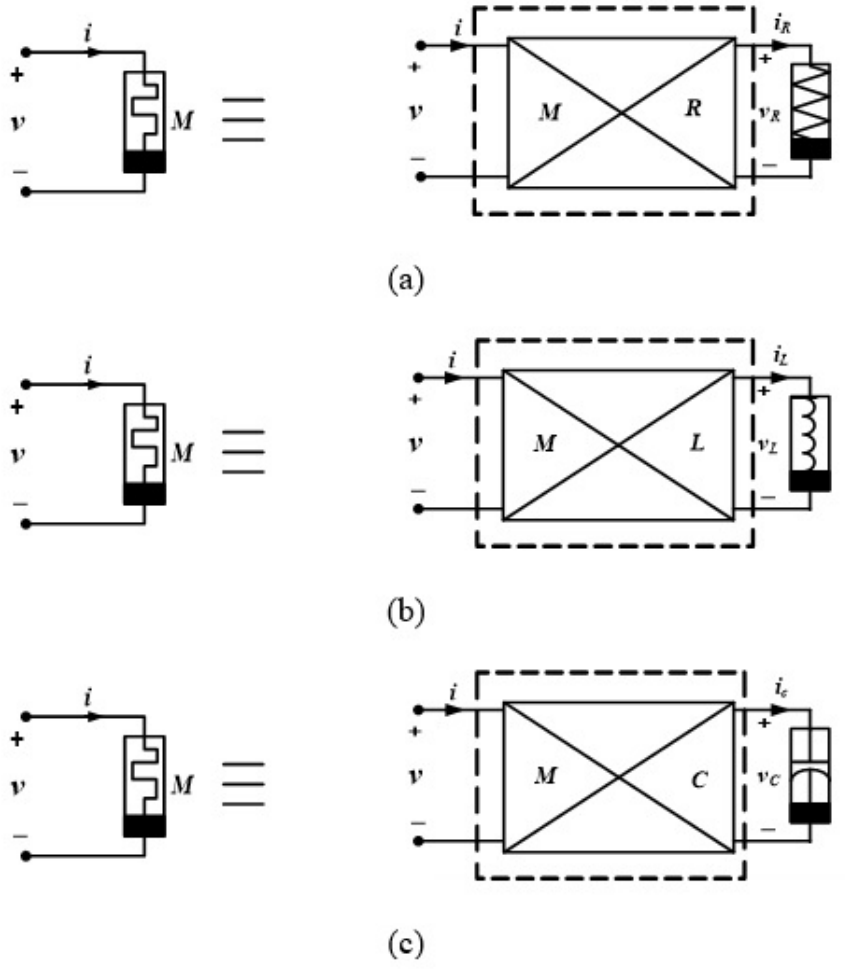


Figure 2.1: (a) M-R mutator (b) M-L mutator (c) M-C mutator.

The M-R, M-L, and M-C mutators which will be presented in this chapter, mutate a resistor or capacitor or inductor, all non-linear into a memristor. The basic principle of these types of mutations is preserving the "shape" of the non-linear characteristic of the R, C and L type elements, which are mutated into the corresponding charge-flux constitutive relation of the memristor.

2.1 Mutators for Mutating Nonlinear Circuit Elements to Memristor

2.1.1 Mutators for Mutating Nonlinear Resistor to Memristor

Two types and four circuit level realization for mutating nonlinear resistors to memristors are proposed by Chua as shown in Table 2.1.

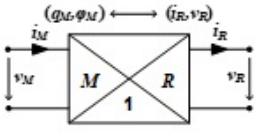
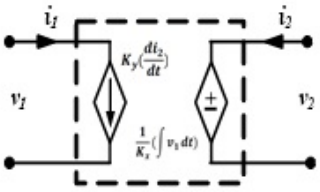
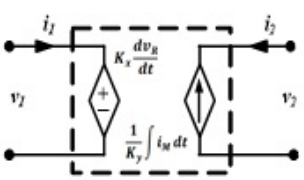
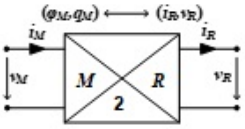
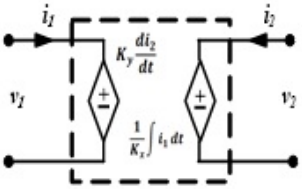
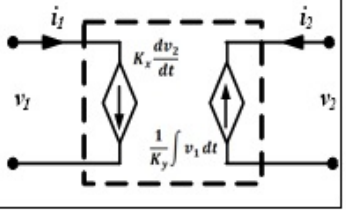
Type	Symbol	Implementation using controlled sources	
		circuit level realization 1	circuit level realization 2
1			
2			

TABLE 2.1: Different circuit level realizations of M-R mutator.

Both type of mutators convert voltage-current characteristic of the nonlinear resistor at port 2 to that of a memristor with same characteristic at port 1 but with a minor difference: for Type-1 v_R-i_R characteristic is mutated to a φ_M-q_M characteristic whereas for Type-2 to that of a q_M-φ_M characteristic.

General definitions of time-invariant nonlinear resistor and memristor are given in (2.1) and (2.2),

$$f_R(v_R, i_R) = 0 \tag{2.1}$$

where v_R, i_R are the voltage and the current of the nonlinear resistor,

$$f_{MR}(\varphi_M, q_M) = 0 \tag{2.2}$$

where q_M, φ_M are the electric charge and flux of the memristor respectively.

In type one, the similarity of characteristics (2.1) and (2.2) can be observed by a linear transformation (a scaling to be more precise) of the coordinates as in (2.3).

$$\begin{cases} q_M = K_y.i_R \\ \varphi_M = K_x.v_R \end{cases} \tag{2.3}$$

In type two, the similarity of characteristics (2.1) and (2.2) can be observed by linear transformations of the coordinates as in (2.4).

$$\begin{cases} q_M = K_x.v_R \\ \varphi_M = K_y.i_R \end{cases} \tag{2.4}$$

where K_x and K_y are real constants with values depending on how the mutator is designed.

The first nonlinear resistor to memristor mutator circuit is shown in Figure 2.2. The M-R mutator of type 1, circuit level realization 1, was selected in [1]. In the circuit implementation of this mutator two operational amplifiers, 14 transistors, and a number of passive components were employed.

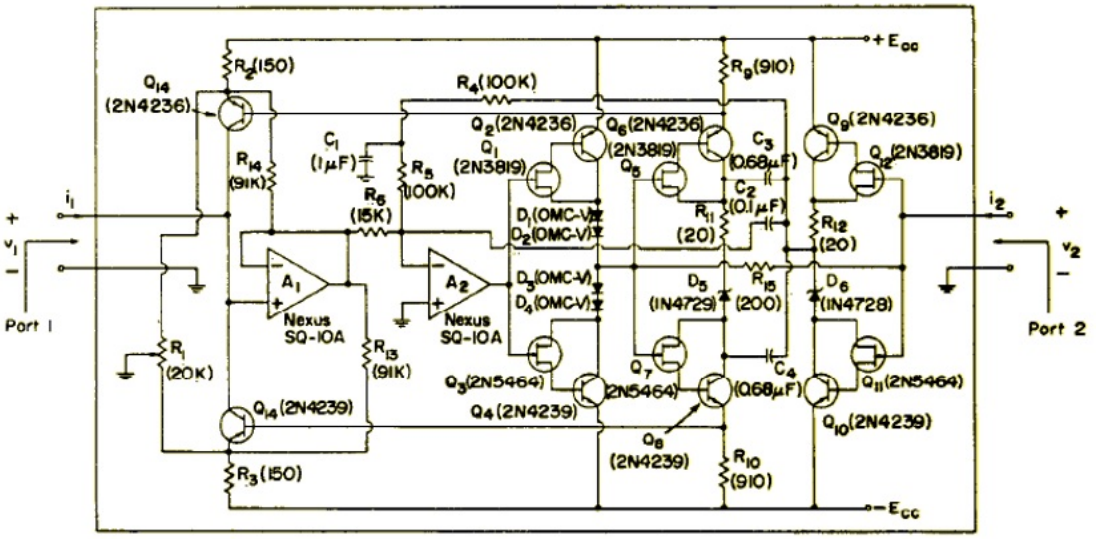


Figure 2.2: The proposed memristor emulator circuit by L.Chua [1].

In 2011 Biolek and Biolkova, by using off-the-shelf components like one Operational Amplifier (OpAmp) and two Current Feedback Operational Amplifiers (CFOA), and several passive elements introduced a mutator circuit shown in Figure 2.3 for mutating nonlinear resistors into memristors [10].

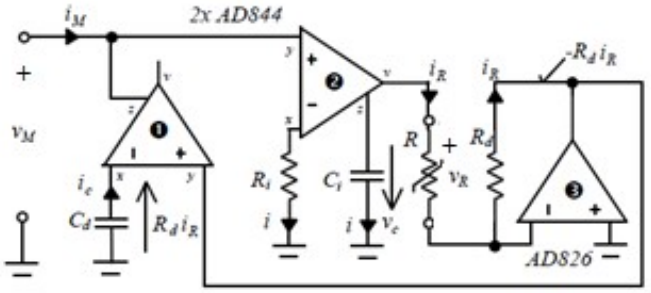


Figure 2.3: Implementation of M-R mutator with two CFOAs and one OpAmp

In 2014 a grounded memristor emulator circuit including three CFOAs, two resistors, two capacitors and one nonlinear resistor was presented in [110]. The circuit structure is shown in Figure 2.4.

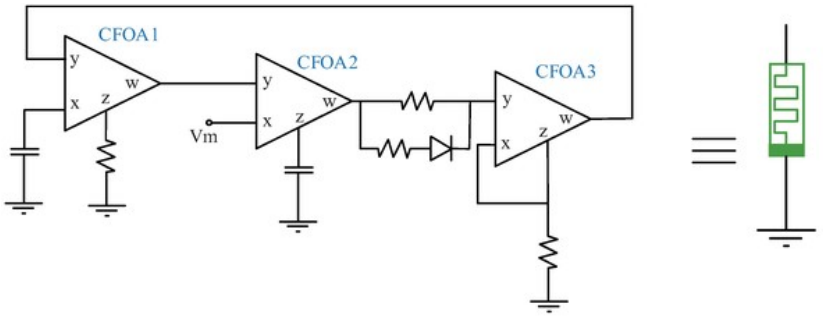


Figure 2.4: Circuit structure of grounded memristor emulator in [110]

2.1.2 Mutators for Mutating Nonlinear-Inductor to Memristor

Two types and six circuit level realizations for mutating nonlinear inductor to memristor are proposed by Chua in [1], as shown in Table 2.2.

Both type of mutators convert φ_L-i_L characteristic of the time-invariant nonlinear-inductor at port two to that of a memristor with same characteristic at port one

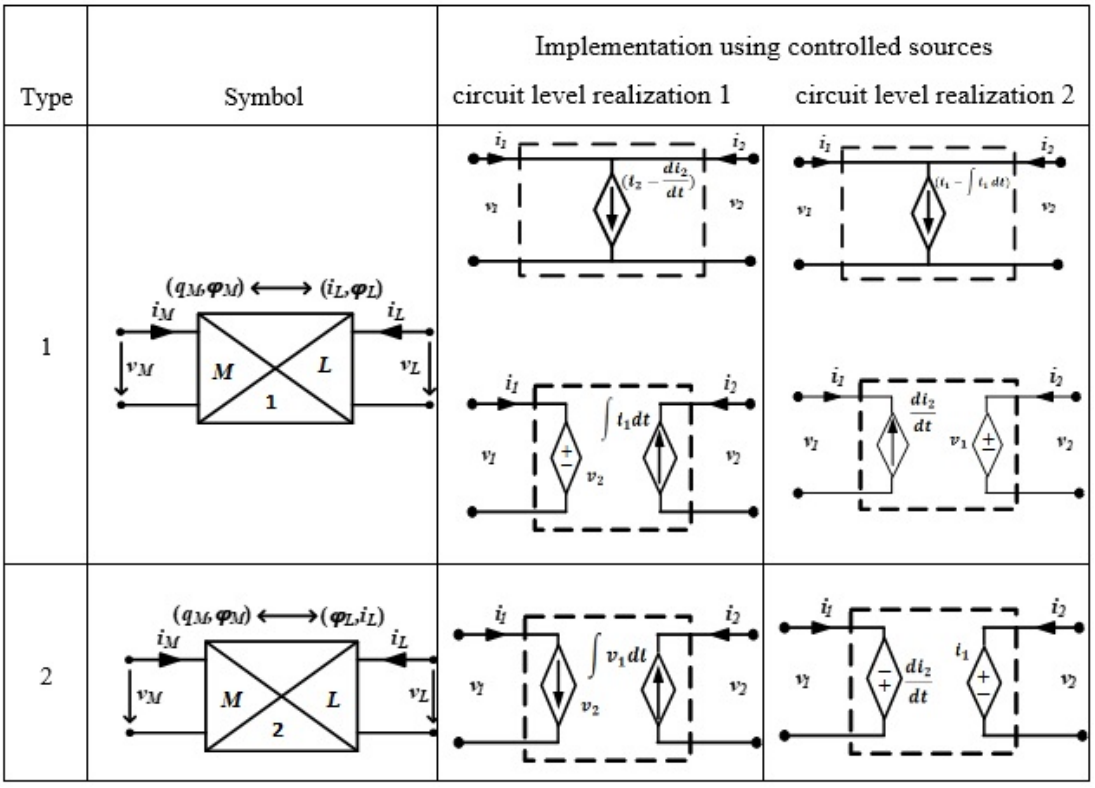


TABLE 2.2: Two types and six circuit level realizations of M-L mutators.

but with a minor difference: for Type-1 φ_L-i_L characteristic is mutated to a φ_M-q_M whereas for Type-2 to that of a q_M-φ_M characteristic.

In the sequel some generalized 4-ports will be so designed that both types of mutators can be obtained with proper termination of two of the ports.

General definitions of time-invariant nonlinear-inductor and memristor are given with:

$$f_L(i_L, \varphi_L) = 0 \tag{2.5}$$

where i_L, φ_L are current and flux of the nonlinear-inductor respectively.

$$f_{MR}(q_M, \varphi_M) = 0 \tag{2.6}$$

where q_M-φ_M are charge and flux of the memristor respectively.

In type one, the similarity of characteristics (2.5) and (2.6) can be observed by linear transformations of the coordinates as in (2.7).

$$\begin{cases} \varphi_L = K_x.\varphi_M \\ i_L = K_y.q_M \end{cases} \tag{2.7}$$

In type two, the similarity of characteristics (2.5) and (2.6) can be observed by linear transformations of the coordinates as in (2.8).

$$\begin{cases} \varphi_L = K_x.q_M \\ i_L = K_y.\varphi_M \end{cases} \tag{2.8}$$

where K_x and K_y are real constants with values depending on how the mutator is designed.

2.1.3 Mutators for Mutating Nonlinear-Capacitor to Memristor

Two types and six circuit level realizations for mutating a time-invariant nonlinear-capacitor to a memristor proposed by Chua in [1] are shown in Table 2.3.

Both type of mutators convert the q_C-v_C characteristic of the time-invariant nonlinear-capacitor at port two to that of a memristor with the same characteristic at port one but with a minor difference: for Type-1 q_C-v_C characteristic is mutated to a q_M-φ_M whereas for Type-2 to that of a φ_M-q_M characteristic. In the sequel a generalized mutative 4-port will be so designed that all types of mutators can be obtained with proper termination of two of the ports.

General definitions of nonlinear-capacitor and memristor are given with (2.9) and (2.10) respectively.

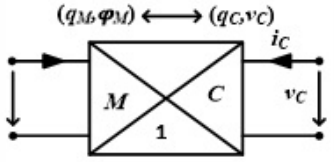
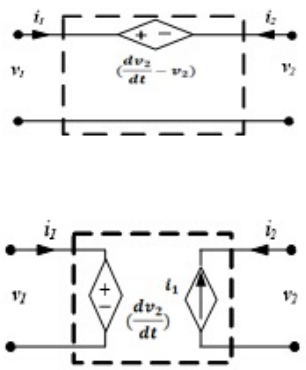
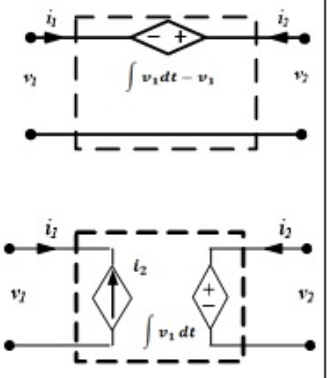
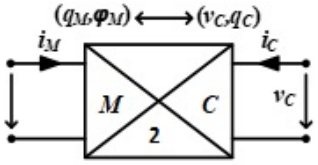
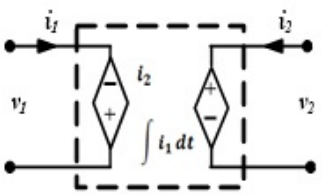
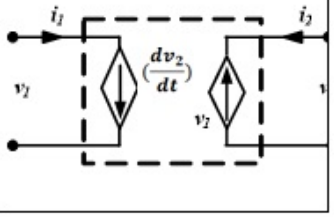
Type	Symbol	Implementation using controlled sources circuit level realization 1	 circuit level realization 2
1			
2			

TABLE 2.3: Two types and six circuit level realizations of M-C mutators.

$$f_C(q_C, v_C) = 0 \tag{2.9}$$

where q_C, v_C are the charge and voltage of the nonlinear-capacitor respectively.

$$f_{MR}(q_M, \varphi_M) = 0 \tag{2.10}$$

where q_M, φ_M are the charge and the flux of the memristor.

In type one, the similarity of characteristics (2.9) and (2.10) can be observed by linear transformations of the coordinates as in (2.11).

$$\begin{cases} q_M = K_x.q_C \\ \varphi_M = K_y.v_C \end{cases} \tag{2.11}$$

In type two, the similarity of characteristics (2.9) and (2.10) can be observed by linear transformations of the coordinates as in (2.12)

$$\begin{cases} q_M = K_x.v_C \\ \varphi_M = K_y.q_C \end{cases} \tag{2.12}$$

where K_x and K_y are real constants with values depending on how the mutator is designed.

2.2 Mutators for Mutating Memristor to Other Memstors

Biolek et al. in 2010, inspired by Chua's mutator circuits, proposed two classes of mutators for mutating memristor to meminductor and memristor to memcapacitor [9]. Each of these classes has two types and four circuit level realizations.

2.2.1 Mutators for Mutating Memristor to Meminductor

The circuit level realizations of ML-MR mutator which are extracted from [9], are illustrated in Table 2.4.

Both type of mutators convert q_M, φ_M characteristic of the memristor at port two to that of a meminductor with the same characteristic at port one but with a minor difference: for Type-1 q_M, φ_M characteristic is mutated to a ρ_L-q_L characteristic whereas for Type-2 to that of a q_L-ρ_L characteristic.

General definitions of memristor and meminductor are given as:

$$f_{MR}(q_M, \varphi_M) = 0 \tag{2.13}$$

where φ_M-q_M are the charge and flux of the memristor respectively.

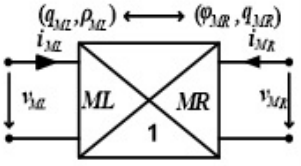
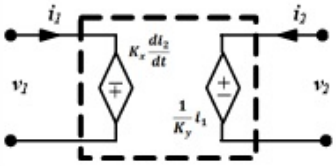
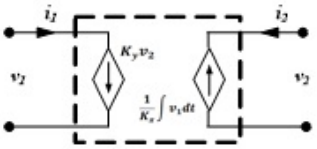
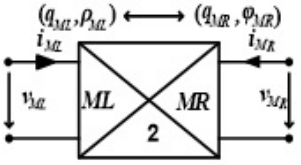
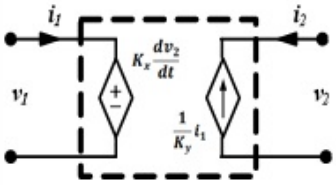
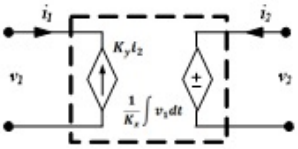
Type	Symbol	Circuit level realization 1	Circuit level realization 2
1			
2			

TABLE 2.4: Two types and four circuit level realizations for ML-MR mutators.

$$f_{ML}(q_L, \rho_L) = 0 \tag{2.14}$$

where q_L and ρ_L are the charge and the time integral of flux of the meminductor.

In type one, the similarity of characteristics (2.13) and (2.14) can be observed by linear transformations of the coordinates as in (2.15).

$$\begin{cases} q_L = K_y.\varphi_M \\ \rho_L = K_x.q_M \end{cases} \tag{2.15}$$

In type two, the similarity of characteristics (2.13) and (2.14) can be observed by linear transformations of the coordinates as in (2.16).

$$\begin{cases} q_L = K_y.q_M \\ \rho_L = K_x.\varphi_M \end{cases} \tag{2.16}$$

where K_x and K_y are real constants with values depending on how the mutators are designed.

2.2.2 Mutators for Mutating Memristor to Memcapacitor

The circuit level realizations of MC-MR mutator, which are extracted from [9], are illustrated in Table 2.5.

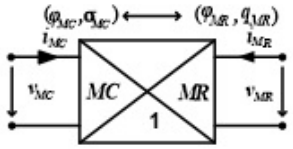
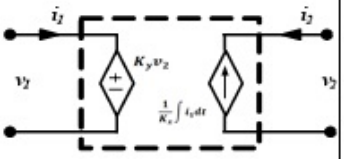
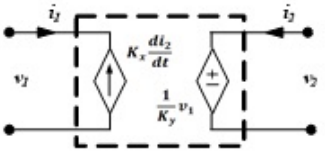
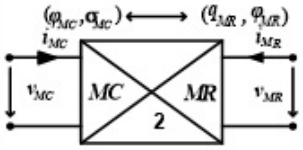
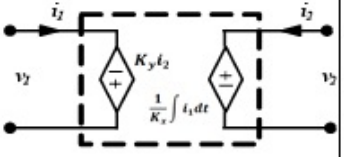
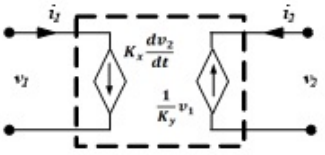
Type	Symbol	circuit level realization 1	circuit level realization 2
1			
2			

TABLE 2.5: Two types and four circuit level realizations for MC-MR mutators

Both type of mutators convert q_M, φ_M characteristic of the memristor at port two to that of a memcapacitor with same characteristic at port one but with a minor difference: for Type-1 φ_M-q_M characteristic is mutated to a φ_C-σ_C whereas for Type-2 to that of a σ_C-φ_C characteristic.

General definitions of memristor and memcapacitor are given as

$$f_{MR}(\varphi_M, q_M) = 0 \tag{2.17}$$

where q_{MR} and φ_{MR} are charge and flux of memristor respectively.

$$f_{MC}(\sigma_C, \varphi_C) = 0 \tag{2.18}$$

where σ_C and φ_C are time integral of charge and flux of memcapacitor.

In type one, the similarity of characteristics (2.17) and (2.18) can be observed by linear transformations of coordinates as in (2.19)

$$\begin{cases} \sigma_C = K_x.q_M \\ \varphi_C = K_y.\varphi_M \end{cases} \tag{2.19}$$

In type two, the similarity of characteristics (2.17) and (2.18) can be observed by linear transformations of coordinates as in (2.20),

$$\begin{cases} \sigma_C = K_x.\varphi_M \\ \varphi_C = K_y.q_M \end{cases} \tag{2.20}$$

Where K_x and K_y are real constants with values depending on how the mutators are designed.

Again in 2010 Pershin and Ventra, by using one OpAmp and several passive components, as shown in Figure 2.5, introduced mutator circuits for realizing lossy meminductors and lossy memcapacitors from memristors [7]. In simulations they have used the memristor emulator circuit in [3] and shown an interesting connection between three memory elements.

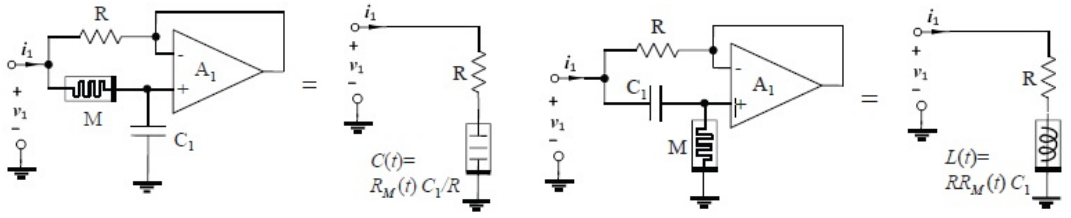


Figure 2.5: Lossy memcapacitor emulator and lossy meminductor emulator

In 2010, Biolek et al., proposed a circuit for converting memristors to memcapacitors by employing two Operational Transconductance Amplifiers (OTAs) and several passive components, [8]; circuit structure is shown in Figure 2.6.

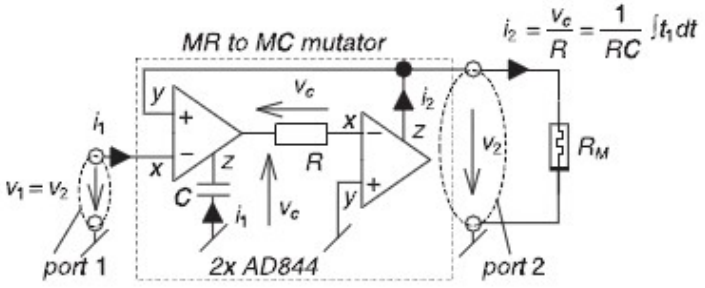


Figure 2.6: MC-MR mutator circuit by Biolek et al.

In 2010 Biolek et al. using one plus type Second Generation Current Conveyor (CCII+) and one OTA proposed mutators which mutate memristors into memcapacitors and meminductors. The proposed metamutator realization is shown in Figure 2.7; the constitutive relation of the memristor is preserved, within scaling, by the elements obtained after the mutation [9].

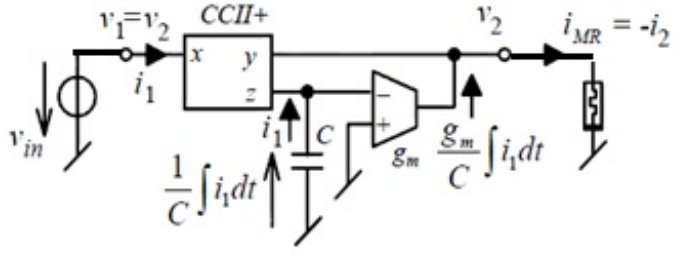


Figure 2.7: MC-MR mutator circuit by Biolek et al.

In 2011 Pershin and Ventra, using four current conveyors (CCII) and several passive elements mutated a memristor to a floating memcapacitor or a meminductor. The circuit implementation is shown in Figure 2.8.

In the same paper, with two dual output current conveyors and several passive components, they proposed other circuits for emulating a floating meminductor and a memcapacitor from a memristor [11]. The circuit structure of these mutators are shown in Figure 2.9.

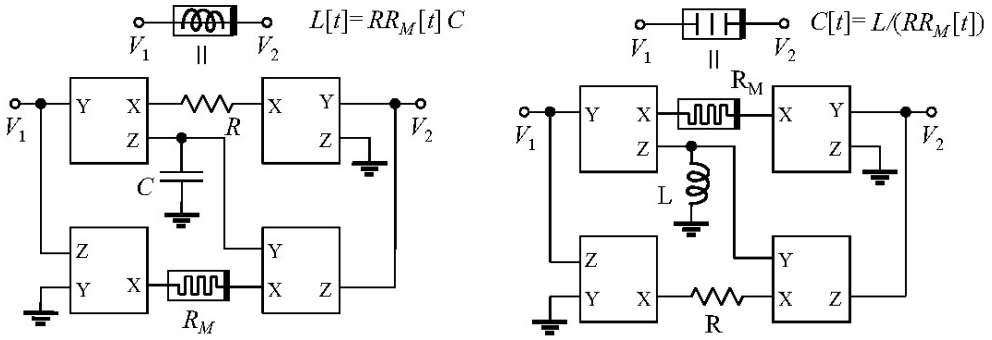


Figure 2.8: CCII based meminductor, memcapacitor emulators [11]

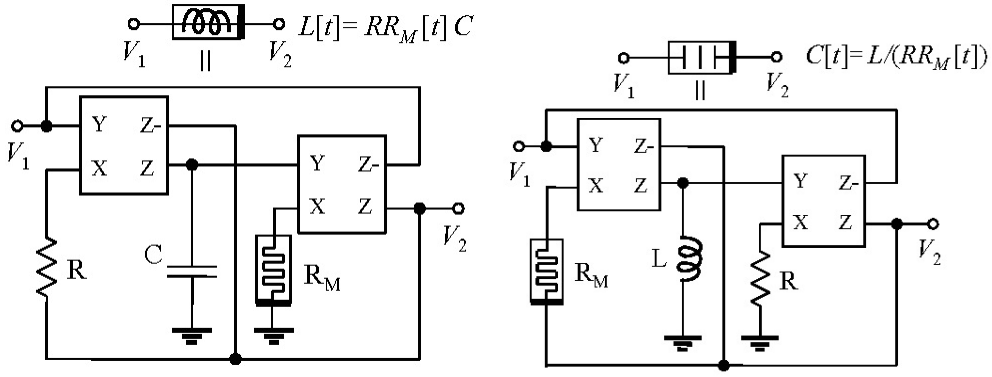


Figure 2.9: Meminductor and memcapacitor emulation with dual-output CCII

Chapter 3

4-Port Metamutators and Their Realizations

3.1 Incognito Presence of Metamutators in Literature

Many electrical circuits, especially those used in realizing emulators/simulators, gyrators, mutators etc. contain, concealed in their complex structure, a sub-circuit which viewed as a 4-port behaves like a Metamutator. Nobody has been able to identify this underlying 4-port and its ability to act as a Metamutator, let alone their diverse applications. In this chapter in addition to introducing some of these incognito metamutator realizations, newly designed metamutator circuits will be presented.

3.1.1 CCII+, CCII- Based Metamutator

In 1970, several new applications of current conveyors were investigated by Sedra and Smith. The circuit shown in Figure 3.1 was introduced in [22] to operate as a gyrator for realizing a grounded inductor.

In the following it will be shown that the 4-port given in Figure 3.2 extracted from the circuit shown in Figure 3.1, behaves like a metamutator by proving that its port description satisfies the defining expression of CIM as given with (1.10).

In the circuit of Figure 3.2 one CCII+ and one CCII- are used. The block diagrams and port description matrices of current conveyors are given below:

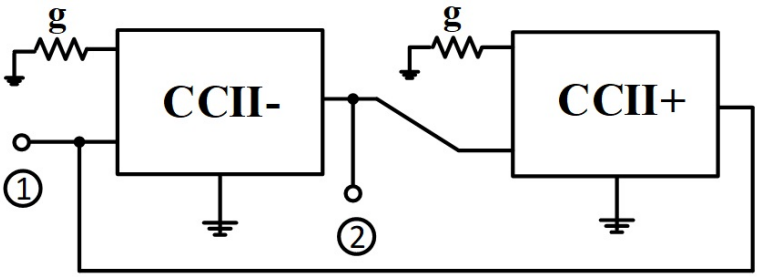


Figure 3.1: The gyrator circuit by Sedra and Smith [22]

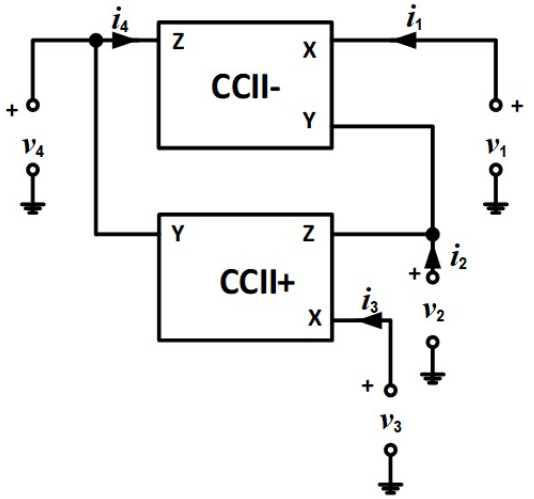


Figure 3.2: Diagram of the metamutator obtained from the gyrator circuit in [22].

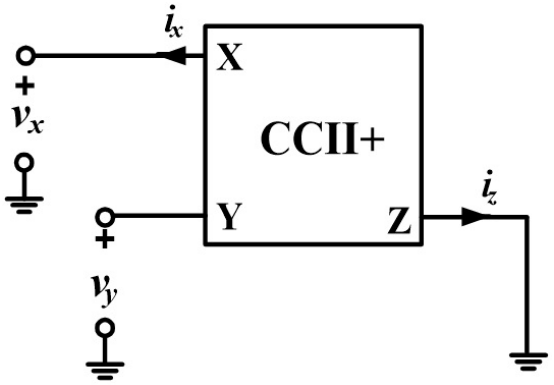


Figure 3.3: Block diagram of CCII+

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \times \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{3.1}$$

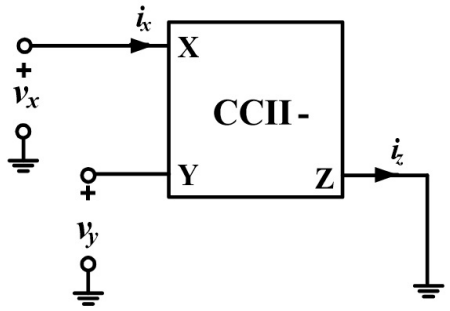


Figure 3.4: Block diagram of CCII-

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & -1 & 0 \end{bmatrix} \times \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{3.2}$$

CMOS realization of CCII+ and CCII- extracted from [23] are shown in Figure 3.5.

Transistor dimensions are given with Table 3.1 and Table 3.2.

MOSFET	W (μm)	L (μm)
M_1, M_2, M_3	50	1.05
M_7, M_8	40	1.05
M_9	120	1.05
M_{10}, M_{11}, M_{12}, M_{13}	20	1.05

TABLE 3.1: Dimension of transistors used in CCII+

MOSFET	W (μm)	L (μm)
M_1, M_2, M_4	50	1.05
M_5, M_6, M_7, M_8	40	1.05
M_9	120	1.05
M_{10}, M_{11}, M_{12}, M_{14}, M_{15}, M_{16}	20	1.05

TABLE 3.2: Dimension of transistors used in CCII-

By applying KVL, KCL and writing a chain of equalities from the description matrices of CCII+ and CCII-, port relation matrix of the 4-port in Figure 3.2 is obtained as:

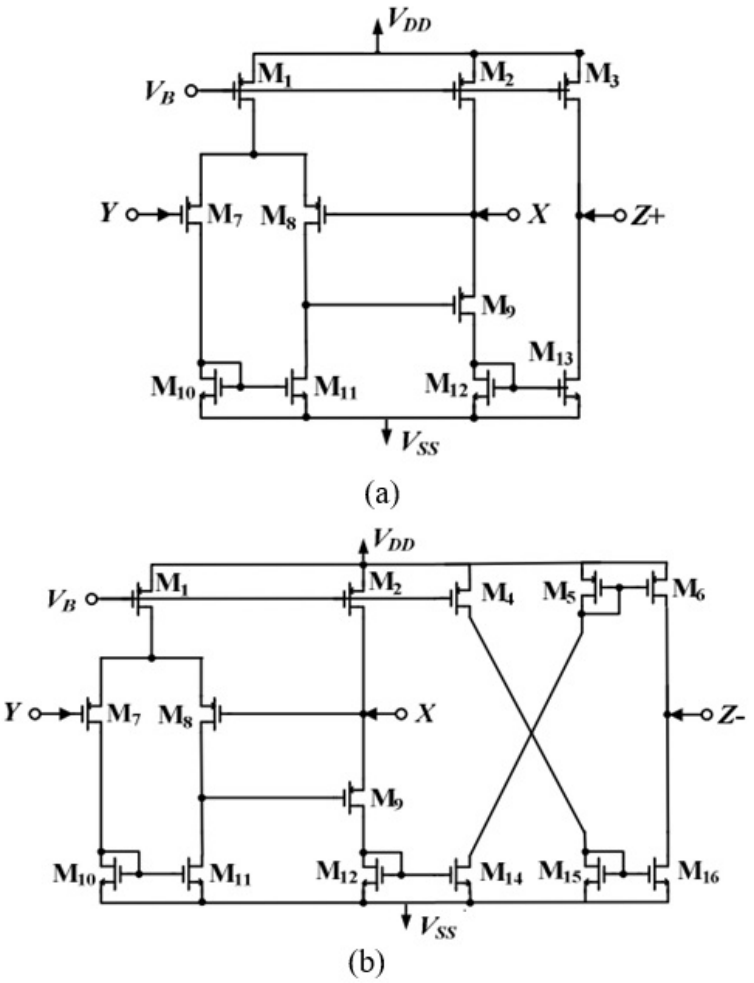


Figure 3.5: CMOS realization of: (a) (CCII+), (b) (CCII-)

$$\begin{bmatrix} i_2 \\ i_4 \\ v_3 \\ v_1 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_3 \\ -i_1 \\ v_4 \\ v_2 \end{bmatrix} \tag{3.3}$$

As one can see the port relation matrix of the 4-port in Figure 3.2 is the same as (1.10), which verifies that the configuration in Figure 3.2 is indeed a CIM. Comparing with (1.9) that $m = 3$, $l = 4$, $n = 1$ and $k = 2$ can be observed.

In the following, the frequency ranges in which the CCII+, CCII- metamutator's

port relations in (3.3) are satisfied, will be investigated. For CCII+ and CCII-, TSMC, 0.35 μm CMOS process parameters were used with transistor dimensions as shown in Table 3.1 and Table 3.2 and their circuits given in Figure 3.5. Supply voltages are chosen as $\pm$1.65V, and V_B as 0.7V.

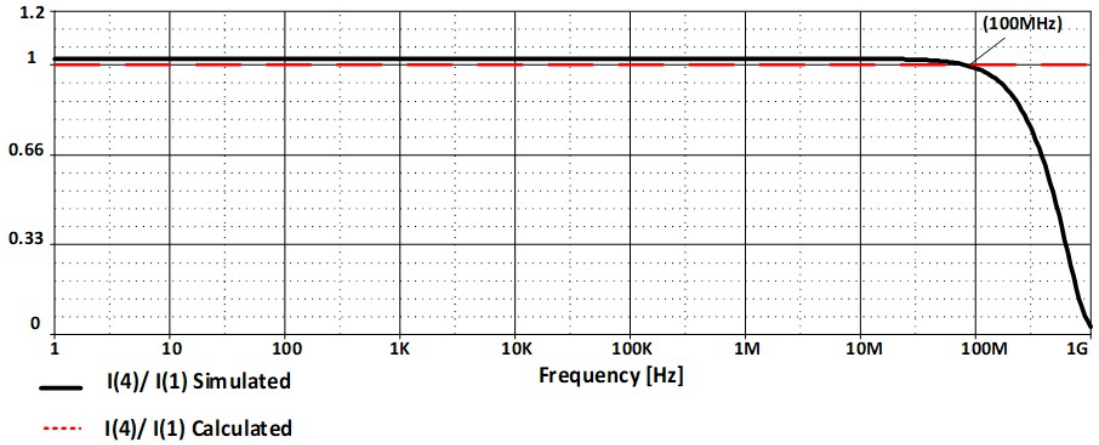


Figure 3.6: Theoretical and simulation characteristics of i_4 vs. i_1

The characteristic in Figure 3.6 is obtained by applying an AC current source with amplitude of 10μA to port 1 and connecting 1Ω resistors to other ports of the metamutator.

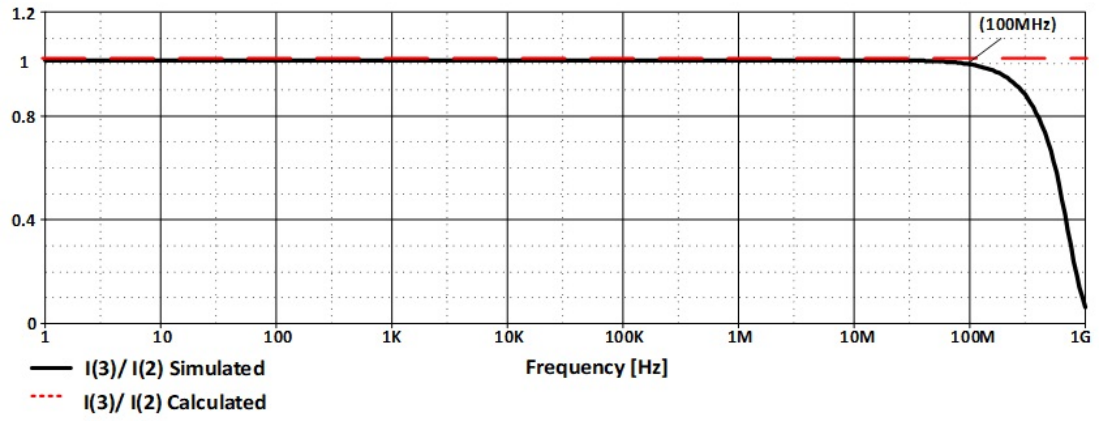


Figure 3.7: Theoretical and simulation characteristics of i_3 vs. i_2

The characteristic in Figure 3.7 is achieved by applying an AC current source with amplitude of 10μA to port 2 and connecting 1Ω resistors to the other ports

of the metamutator. According to simulation results in Figure 3.6 and Figure 3.7, currents match up until 100+MHz which proves that the operation of this metamutator is as desired in a wide range of frequency.

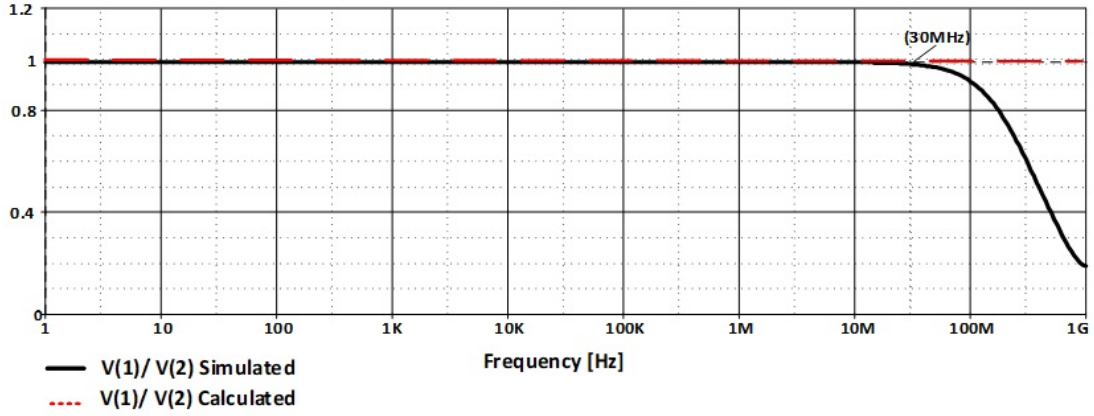


Figure 3.8: Theoretical and simulation characteristics of v_2 vs. v_1

The characteristic in Figure 3.8 is achieved by applying an AC voltage source with 1V amplitude to port 2 and connecting 100kΩ resistors to the other ports of the metamutator.

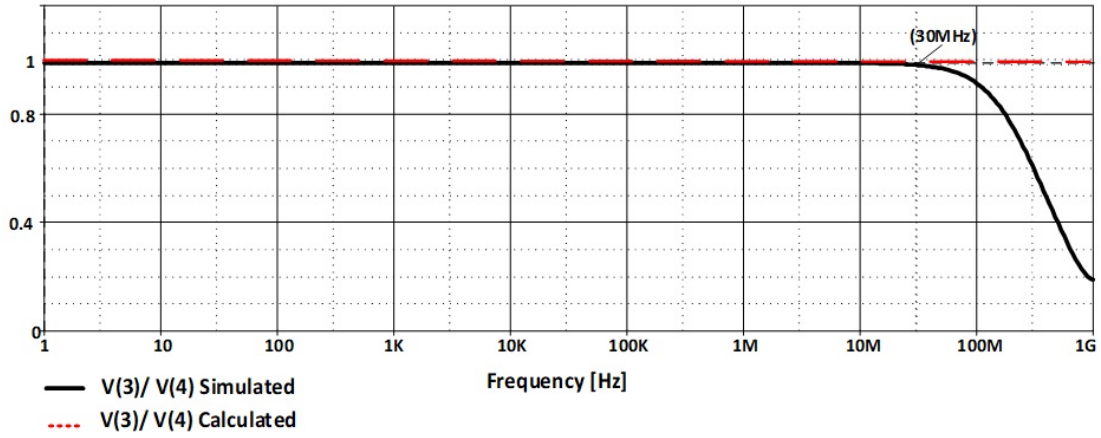


Figure 3.9: Theoretical and simulation characteristics of v_3 vs. v_4

The characteristic in Figure 3.9 is achieved by applying an AC voltage source with 1V amplitude to port 4 and connecting 100kΩ resistors to the other ports of the metamutator.

According to simulation results in Figure 3.8 and Figure 3.9, voltages match up until 50+MHz proving the operation of the metamutator is as desired in a wide range of frequency.

3.1.2 CCII+ and CF Based Metamutator

Another metamutator circuit structure is shown in Figure 3.10. A plus type second generation Current Conveyor (CCII+) and a Current Follower (CF) are employed in the structure of this metamutator.

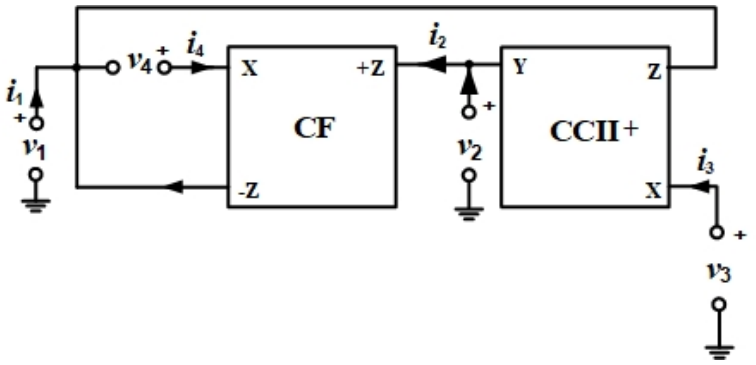


Figure 3.10: Metamutator with CCII+ and CF [27]

First the circuit was present in a configuration built for realizing grounded or floating inductors in [27] but definitely not as a metamutator. Then in [24-26] the circuit was slightly modified for realizing a metamutator. The port diagram and port description matrix of the current follower are given below:

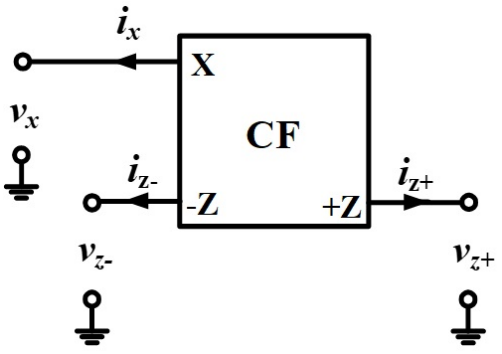


Figure 3.11: Block diagram of CF

$$\begin{bmatrix} v_x \\ i_{z+} \\ i_{z-} \end{bmatrix} = \begin{bmatrix} 0 \\ 1 \\ -1 \end{bmatrix} .i_x \tag{3.4}$$

The CMOS realization of CF extracted from [23] is shown with Figure 3.12

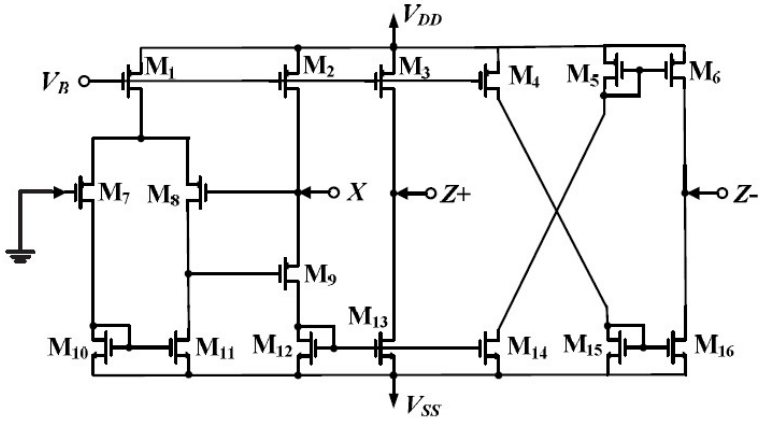


Figure 3.12: CMOS realization of CF

Transistor dimensions are shown in Table 3.3.

MOSFET	W (μm)	L (μm)
M_1, M_2,M_3, M_4	50	1.05
M_5, M_6, M_7, M_8	40	1.05
M_9	120	1.05
M_{10}, M_{11}, M_{12}, M_{13}, M_{14}, M_{15}, M_{16}	20	1.05

TABLE 3.3: Dimension of transistors used in CF

By writing Kirchoff's laws and applying chain of defining equalities (3.1) and (3.4) for CCII+ and CF based metamutator in Figure 3.10, the matrix equality (3.5) is obtained,

$$\begin{bmatrix} i_1 \\ i_2 \\ v_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_3 \\ i_4 \\ v_2 \\ -v_1 \end{bmatrix} \tag{3.5}$$

As one can see the ports relation matrix of 4-port with CCII+ and CF+ is the same as (1.9), so this is a VIM configuration. Comparing with (1.9) gives, $m = 3, l = 2, n = 4$ and $k = 1$.

In the sequel the frequency ranges in which CCII+ and CF based metamutator operates optimally have been investigated. For CCII+ and CF TSMC, 0.35 μm CMOS process parameters were used with transistor dimensions as shown in Table 3.1 and Table 3.3, their circuit in Figure 3.5 (a) and Figure 3.12 and, supply voltages chosen as $\pm$1.65V, and V_B as 0.7V.

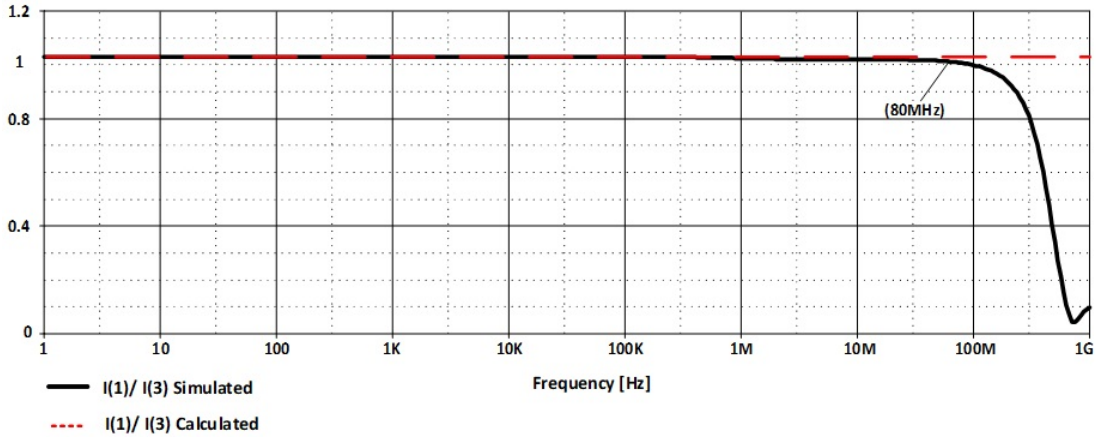


Figure 3.13: Theoretical and simulation characteristics of i_1 vs. i_3

The characteristic in Figure 3.13 is achieved by applying an AC current source with amplitude of 100μA to ports 3 and connecting 1Ω resistors to the other ports of CCII+ and CF based metamutator.

The characteristic in Figure 3.14 is achieved by applying an AC voltage source with amplitude 100μA to ports 4 and connecting 1Ω resistors to the other ports of CCII+ and CF based metamutator.

According to simulation results in Figure 3.13 and Figure 3.14, currents match up until 80MHz and 60MHz respectively, which prove the proper operation of CCII+ and CF based metamutator is as desired in a wide range of frequency.

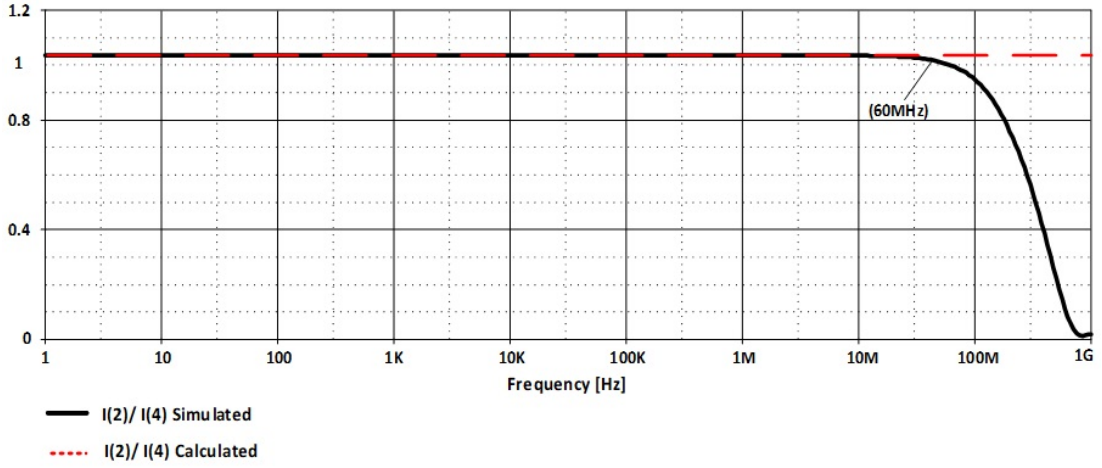


Figure 3.14: Theoretical and simulation characteristics of i_2 vs. i_4

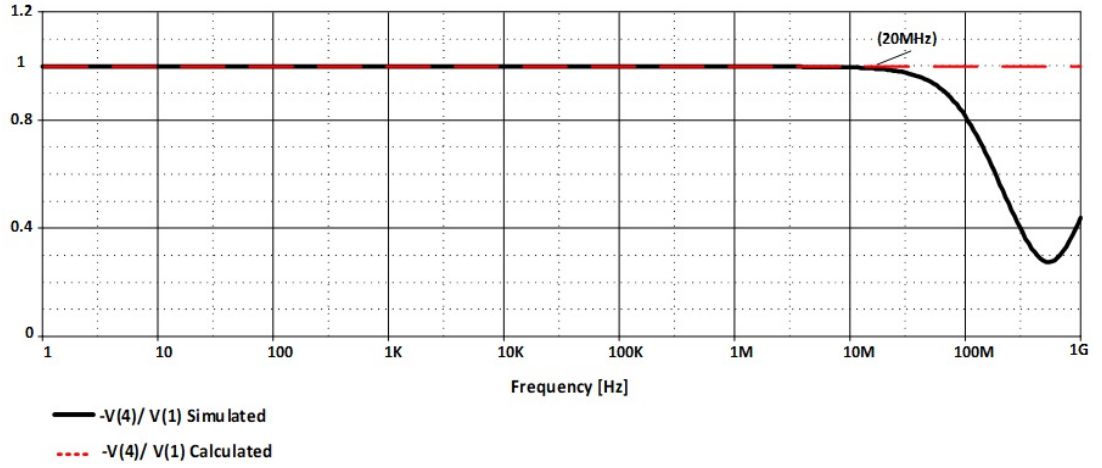


Figure 3.15: Theoretical and simulation characteristics of v_4 vs. v_1

The characteristic in Figure 3.15 is achieved by applying an AC voltage source with amplitude of 1V to port 1 and connecting 100kΩ resistors to the other ports of CCII+ and CF based metamutator.

The characteristic in Figure 3.16 is achieved by applying an AC voltage source with amplitude of 1V to port 2 and placing 100kΩ resistors to the other ports of CCII+ and CF based metamutator.

According to simulation results in Figure 3.15 and Figure 3.16, voltages match up until 20MHz for both characteristics which prove the operation of metamutator

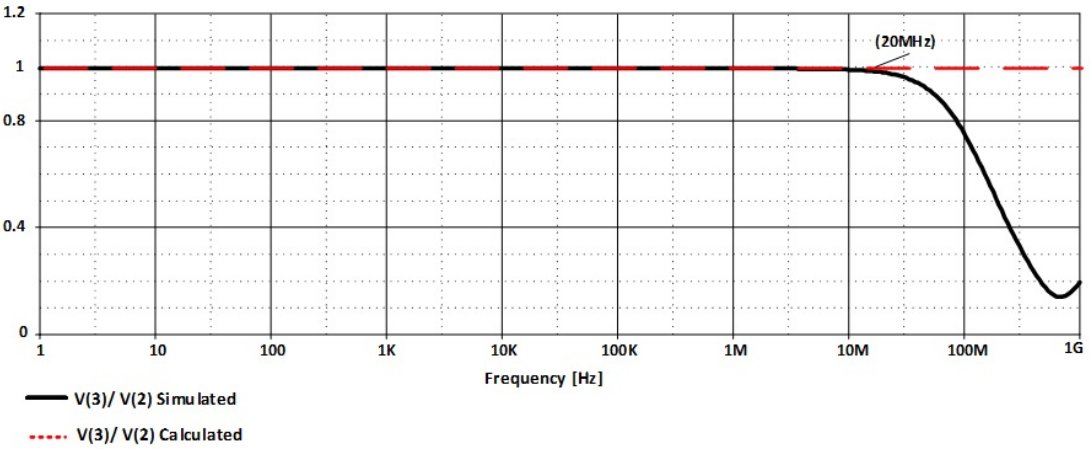


Figure 3.16: Theoretical and simulation characteristics of v_3 vs. v_2

with CCII+ and CF is as desired in a wide range of frequency.

3.1.3 CCII+ Based Metamutator

The circuit in Figure 3.17 was first introduced by Ferri for the purpose of simulating a floating inductor [82].

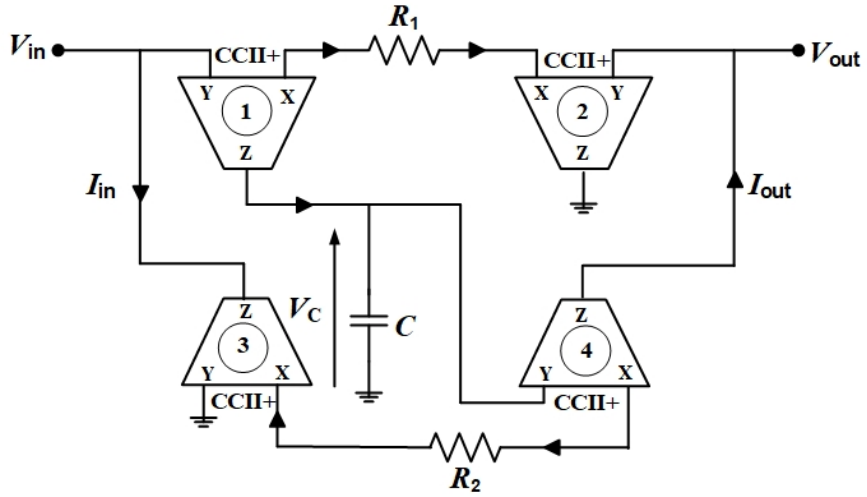


Figure 3.17: CCII+ based inductor simulator proposed in [82]

In the following it will be shown that the 4-port given in Figure 3.18 extracted from the circuit shown in Figure 3.17, behaves like a metamutator by proving that its port description satisfies the defining expression of VIM as given in (1.9).

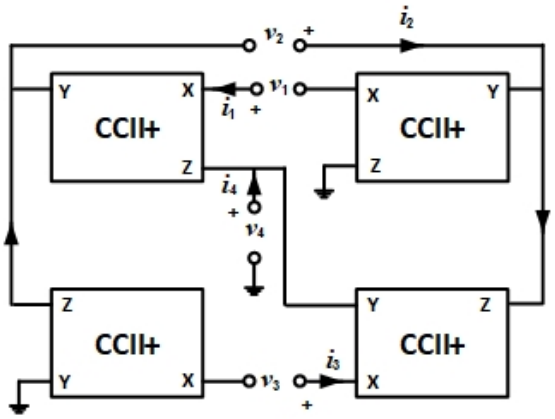


Figure 3.18: Diagram of metamutator extracted from [82]

In the circuit of Figure 3.18 four plus type second generation current conveyors are used. The block diagram and port description matrix of the current conveyor are presented in Figure 3.3 and (3.1).

By applying KVL, KCL and writing a chain of equalities from the description matrix of CCII+, port relation matrix of the 4-port in Figure 3.18 will be obtained as:

$$\begin{bmatrix} i_4 \\ i_2 \\ v_1 \\ v_3 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_1 \\ i_3 \\ -v_2 \\ v_4 \end{bmatrix} \tag{3.6}$$

As one can see the ports relation matrix of the meminductor simulator configuration in [82] is the same as (1.9) which verifies that the configuration in Figure 3.18 is indeed a VIM. Comparing with (1.9), $m = 3, l = 4, n = 1$ and $k = 2$ is observed.

In the following, the frequency ranges in which CCII+ based metamutator operates optimally is investigated. For CCII+ TSMC, 0.35μm CMOS process parameters were used with transistor dimensions as shown in Table 3.1 and its circuit as in Figure 3.5 (a). supply voltages chosen as $\pm$1.65V, and V_B as 0.7V.

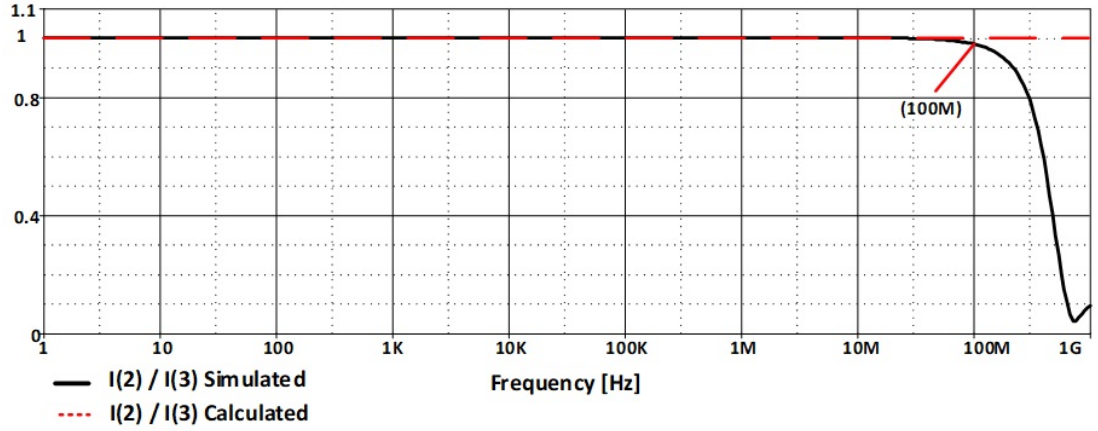


Figure 3.19: Theoretical and simulation characteristics of i_2 vs. i_3

The characteristic in Figure 3.19 is obtained by applying an AC current source with amplitude of 100μA to port 3 and connecting 1Ω resistors to the other ports of CCII+ based metamutator.

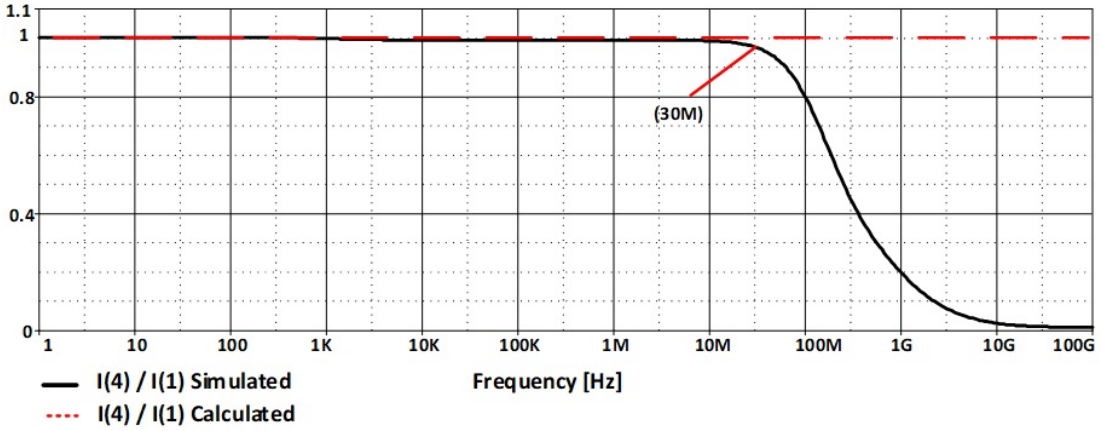


Figure 3.20: Theoretical and simulation characteristics of i_1 vs. i_4

The characteristic in Figure 3.20 is achieved by applying an AC current source with amplitude of 100μA to port 1 and connecting 1Ω resistors to the other ports of CCII+ based metamutator.

According to Simulation results in Figure 3.19 and Figure 3.20 currents match up until 100MHz and 30MHz respectively which prove the operation of CCII+ based metamutator is as desired in a wide range of frequency.

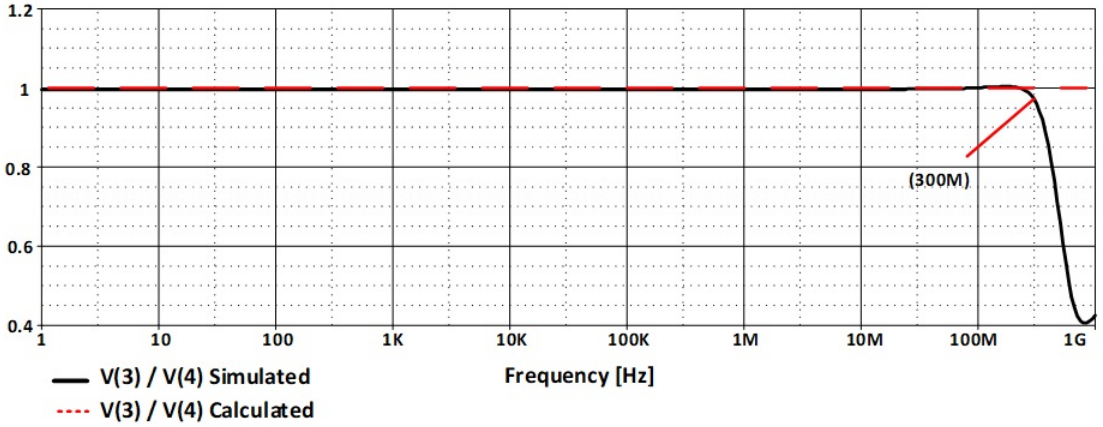


Figure 3.21: Theoretical and simulation characteristics of v_3 vs. v_4

The characteristic in Figure 3.21 is achieved by applying an AC voltage source with amplitude of 1V to port 4 and replacing 100kΩ resistors in the other ports of CCII+ based metamutator.

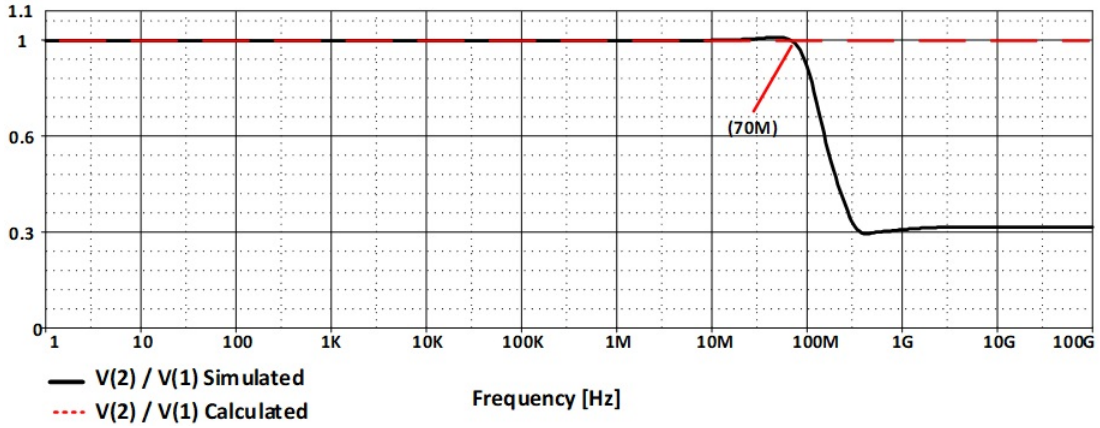


Figure 3.22: Theoretical and simulation characteristics of v_2 vs. v_1

The characteristic in Figure 3.22 is achieved by applying an AC voltage source with amplitude of 1V to port 2 and connecting 100kΩ resistors to the other ports of CCII+ based metamutator.

According to simulation results in Figure 3.21 and Figure 3.22, voltages match up until 300MHz and 70MHz respectively which prove the operation of CCII+ based metamutator is as desired in a wide range of frequency.

3.1.4 Adder and Subtractor Metamutator

Another metamutator configuration is shown in Figure 3.23. As one can see one adder and one subtractor blocks are used in the structure of this circuit. The circuit first was introduced in [4] for realizing a memristor but, not called a metamutator and then in [24-26], it was modified for the purpose of obtaining a 4-port metamutator.

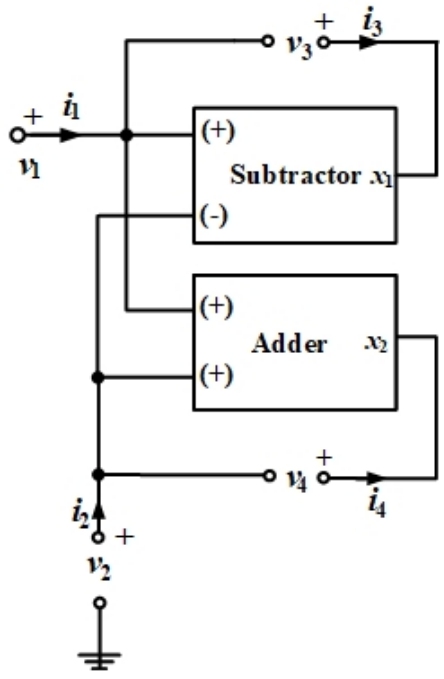


Figure 3.23: Generalized 4-port mutator with adder and subtractor [24-26]

Ideal block diagrams and port relations of adder and subtractor are shown in Fig. 3.24 (a) and (b) respectively,

By writing Kirchoff's laws and applying chain of equalities using the port relations of Adder and Subtractor in Figure 3.23, the matrix equality (3.7) is obtained,

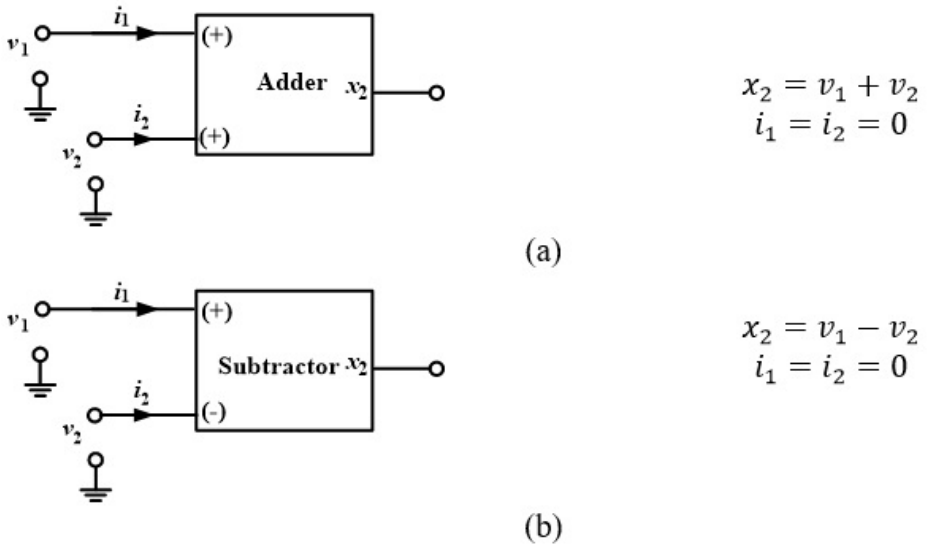


Figure 3.24: Block diagrams and defining relations of (a) adder, (b) subtractor.

$$\begin{bmatrix} i_3 \\ i_4 \\ v_1 \\ v_2 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_1 \\ i_2 \\ v_4 \\ -v_3 \end{bmatrix} \tag{3.7}$$

As one can see the ports relation matrix of 4-port with Adder and Subtractor is the same as (1.9), so this is a VIM configuration. Comparing with (1.9) gives, $m = 1, l = 4, n = 2$ and $k = 3$. Next, the frequency range in which the metamutator with adder and subtractor operates as defined with (3.7) is investigated. As adder and subtractor circuits the CMOS realization with 0.25μm technology with the same transistor dimensions and supply voltages introduced in [4] are used.

The characteristic in Figure 3.25 is achieved by applying an AC current source with amplitude of 10μA to ports 2 and connecting 1Ω resistors to the remaining ports of metamutator with adder and subtractor.

The characteristic in Figure 3.26 is reached by applying an AC current source with amplitude of 10μA to ports 2 and connecting 1Ω resistors to the other ports of metamutator with adder and subtractor.

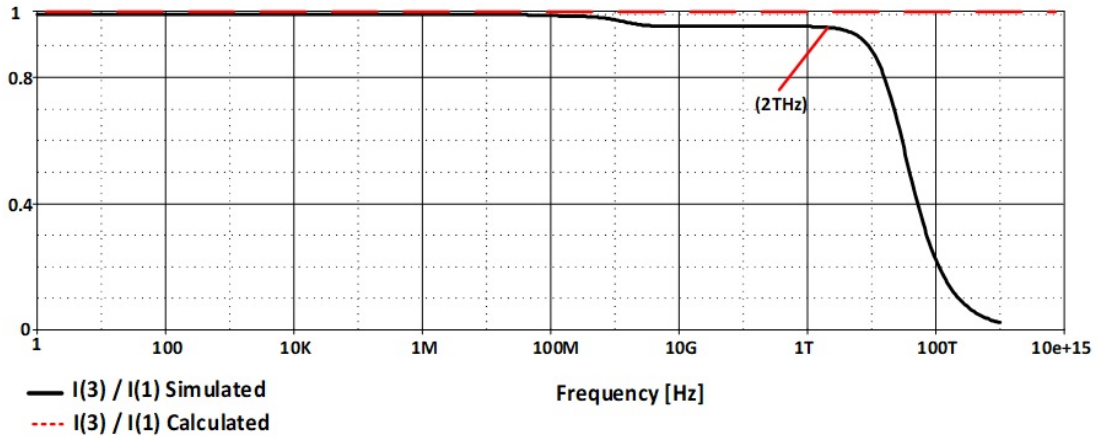


Figure 3.25: Theoretical and simulation characteristics of i_3 vs. i_1

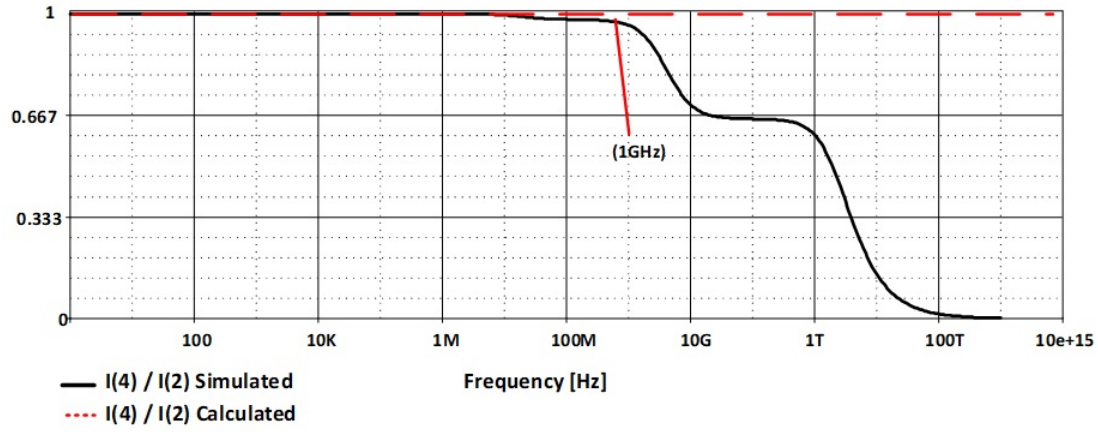


Figure 3.26: Theoretical and simulation characteristics of i_4 vs. i_2

According to simulation results in Figure 3.25 and Figure 3.26, currents match up until 2THz and 1GHz respectively which prove the operation of metamutator with adder and subtractor is as desired in a wide range of frequency.

The characteristic in Figure 3.27 is reached by applying an AC voltage source with amplitude of 1V to ports 1 and attaching 100kΩ resistors to the other ports of metamutator with adder and subtractor.

The characteristic in Figure 3.28 is obtained by applying an AC voltage source with amplitude of 1V to ports 2 and connecting 100kΩ resistors to the other ports of metamutator with adder and subtractor.

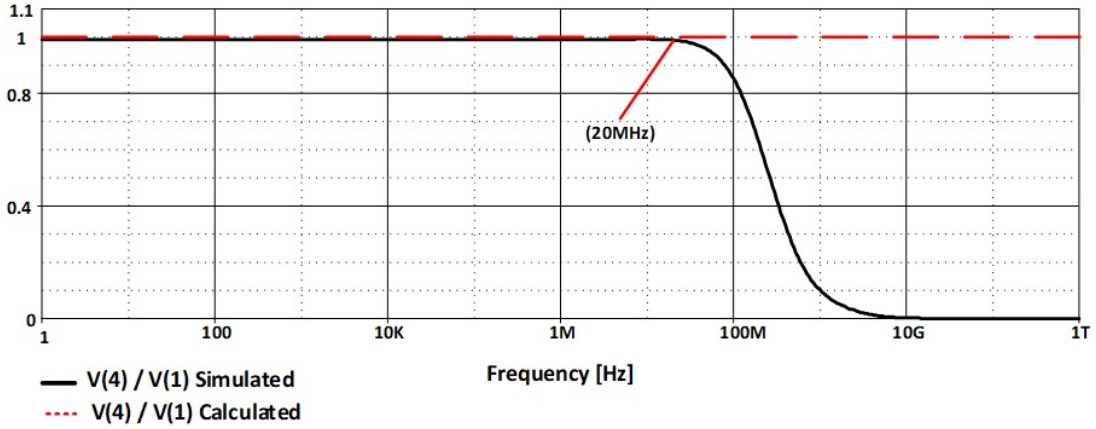


Figure 3.27: Theoretical and simulation characteristics of v_4 vs. v_1

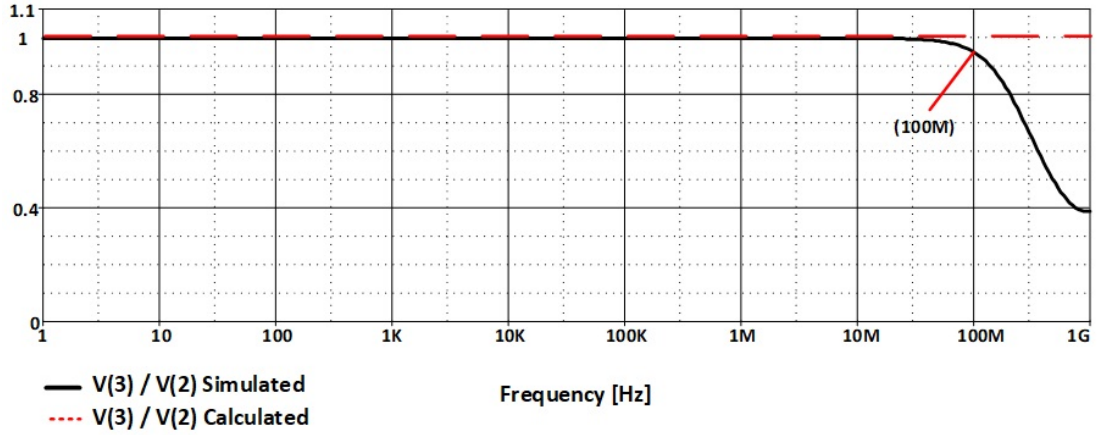


Figure 3.28: Theoretical and simulation characteristics of v_3 vs. v_2

According to simulation results in Figure 3.27 and Figure 3.28 voltages match up until 20MHz and 100MHz respectively which prove the operation of metamutator with adder and subtractor is as desired in a wide range of frequency.

3.2 New Designs for Metamutators with Two Active Devices

In this section three newly designed metamutators using two active blocks each, are being proposed.

3.2.1 Realization with One CFOA and One CCII+

The first metamutator configuration is built using one Current Feedback Operational Amplifier (CFOA) and one second-generation plus type Current Conveyor (CCII+) as illustrated in Figure 3.29.

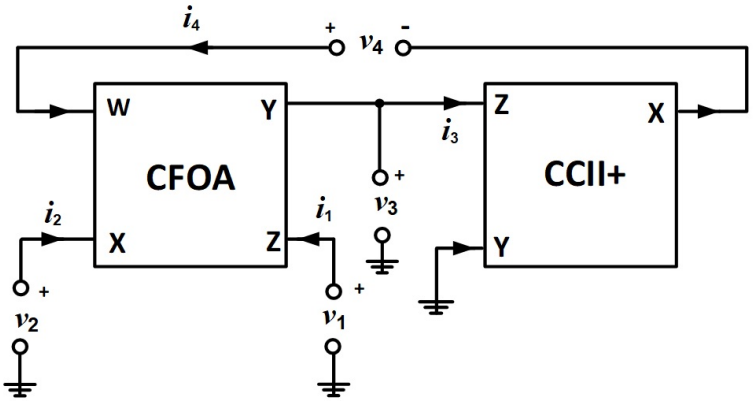


Figure 3.29: Metamutator using CFOA and CCII+

The port definition of ideal CCII+ and CFOA elements are given with matrix representations as shown in (3.8) and (3.9) respectively.

$$\begin{bmatrix} i_y \\ v_x \\ i_z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \times \begin{bmatrix} v_y \\ i_x \\ v_z \end{bmatrix} \tag{3.8}$$

$$\begin{bmatrix} i_z \\ v_x \\ v_w \\ i_y \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \\ 0 & 0 & 0 \end{bmatrix} \times \begin{bmatrix} i_x \\ v_y \\ v_z \end{bmatrix} \tag{3.9}$$

The following chain of equalities is obtained using port descriptions of CFOA and CCII+ and applying Kirchoff's Laws

$$v_2 = v_{(x_1)} = v_{(y_1)} = v_3 \quad \rightarrow \quad v_2 = v_3$$
$$v_1 = v_{(z_1)} = v_{(w_1)} = v_4 - v_{(x_2)} = v_4 - v_{(y_2)} \quad \rightarrow \quad v_4 = v_1$$
$$i_2 = i_{(x_1)} = i_{(z_1)} = i_1 \quad \rightarrow \quad i_1 = i_2$$
$$i_3 = i_{(z_2)} = i_{(x_2)} = -i_4 \quad \rightarrow \quad i_3 = -i_4$$

So the ports description matrix of Figure 3.29 is obtained as,

$$\begin{bmatrix} i_1 \\ i_3 \\ v_2 \\ v_4 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_2 \\ -i_4 \\ v_3 \\ v_1 \end{bmatrix} \tag{3.10}$$

Comparison with (1.9) verifies the existence of CIM configuration. In this case $n = 4, l = 3, m = 2$ and $k = 1$.

3.2.2 Realization with Two DOCCII

The second metamutator configuration is designed by using two Dual Output Current Conveyors (DOCCII) as illustrated in Figure 3.30.

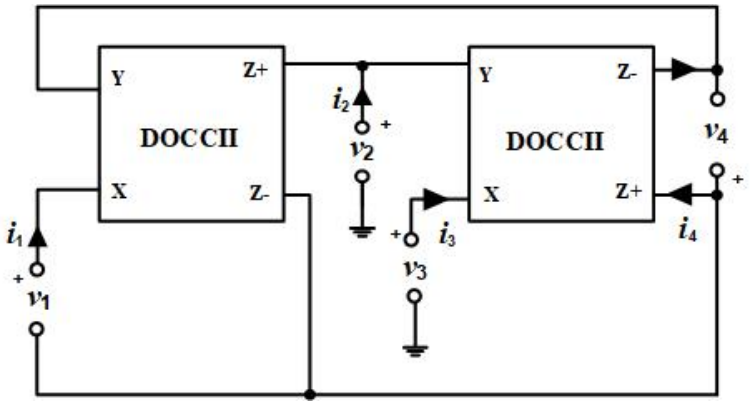


Figure 3.30: Metamutator with two DOCCIIs

The port definition of ideal DOCCII element is given with the matrix representation shown in (3.11),

$$\begin{bmatrix} i_{z+} \\ i_{z-} \\ v_x \\ i_y \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 0 \end{bmatrix} \times \begin{bmatrix} i_x \\ v_y \\ v_z \end{bmatrix} \tag{3.11}$$

Again, the relation between currents and voltages of the ports in the circuit of Figure 3.30, after some algebraic manipulations becomes as given with expression (3.12).

$$\begin{bmatrix} i_4 \\ i_2 \\ v_3 \\ v_1 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_3 \\ i_1 \\ v_2 \\ -v_4 \end{bmatrix} \tag{3.12}$$

Comparison with (1.9) confirms the existence of VIM configuration. In this case $n = 1, k = 4, l = 2$ and $m = 3$.

3.2.3 Realization with Two CFOA

The third metamutator is designed by using two Current Feedback Operational Amplifiers (CFOA) as illustrated in Figure 3.31.

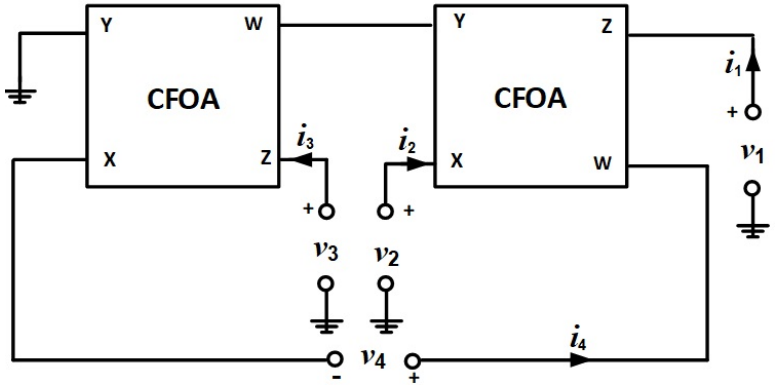


Figure 3.31: Metamutator realized with two CFOAs

The port definition of ideal CFOA element is given with the matrix representation as shown in (3.9). Again, after some algebraic manipulations the relations between currents and voltages of the ports in metamutator shown in Figure 3.31, become as given with expression (3.13).

$$\begin{bmatrix} i_1 \\ i_3 \\ v_2 \\ v_4 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_2 \\ -i_4 \\ v_3 \\ v_1 \end{bmatrix} \tag{3.13}$$

Comparing with (1.10) verifies the existance of CIM configuration. In this case $n = 4, k = 1, l = 3$ and $m = 2$.

3.3 New Designs of Metamutators with Single Active Device

In this chapter three newly proposed metamutator configurations employing only one active devices will be presented. By properly interconnecting the terminals of active devices a Metamutator will be obtained without use of any other external element.

It maintains the following advantages:

i. Use of only one active element, less is the number of active devices less is the amount of disparity

ii. Possibility of realizing Capacitors, Inductors, Memristors, Frequency Dependent Negative Resistor (FDNR), which can be used to make integrated circuits and active filters

iii. No need to impose component choice constraints.

3.3.1 Realization with Negative Type Fully Differential Current Conveyor (FDCCII-)

One of the newly proposed Metamutator configurations employs only one Negative Type Fully Differential Current Conveyor (FDCCII-) which has 9 terminals including ground. By properly interconnecting the terminals of FDCCII- two different types of Metamutator will be obtained without use of any other external element.

The block diagram of the FDCCII- is shown in Figure 3.32.

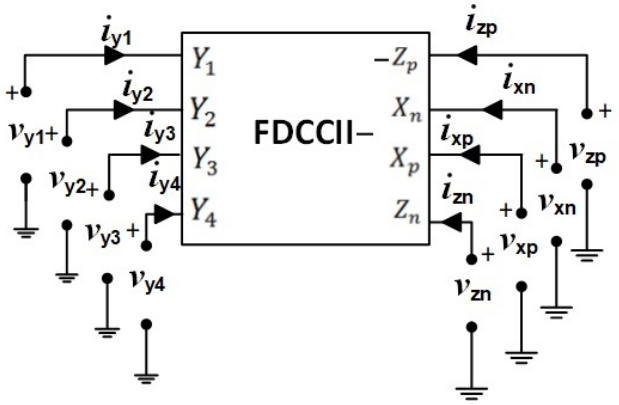


Figure 3.32: Block diagram of FDCCII-

The port description matrix of FDCCII- is,

$$\begin{bmatrix} v_{xp} \\ v_{xn} \\ i_{zp} \\ i_{zn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 1 & -1 & 1 & 0 \\ 0 & 0 & -1 & 1 & 0 & 1 \\ -1 & 0 & 0 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 & 0 & 0 \end{bmatrix} \times \begin{bmatrix} i_{xp} \\ i_{xn} \\ v_{y1} \\ v_{y2} \\ v_{y3} \\ v_{y4} \end{bmatrix} \tag{3.14}$$

And $i_{y1} = i_{y2} = i_{y3} = i_{y4} = 0$.

The CMOS realization of FDCCII- extracted from [84] is shown below.

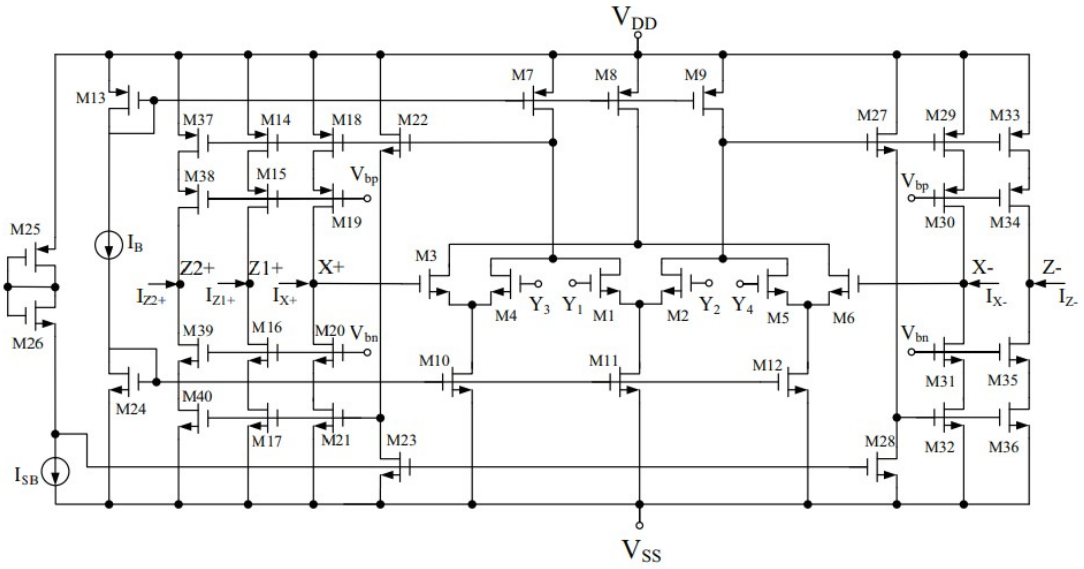


Figure 3.33: CMOS realization of FDCCII- [84]

MOSFET	W (μm)	L (μm)
M_1, M_2,M_4, M_5, M_6	0.7	8.75
M_7, M_8, M_9, M_{13}	0.7	70
M_{10}, M_{11}, M_{12}, M_{24}	0.7	17.5
M_{14}, M_{15},M_{18}, M_{19}, M_{25}, M_{29}, M_{30},M_{33}, M_{34}, M_{37}, M_{38}	0.35	35
M_{16}, M_{17},M_{20}, M_{21}, M_{26}, M_{31}, M_{32},M_{35}, M_{36}, M_{39}, M_{40}	0.35	8.75
M_{22}, M_{23}, M_{27}, M_{28}	0.7	0.7

TABLE 3.4: Dimension of transistors used in FDCCII-

With proper interconnections of port branches as shown in Figure 3.34 and Figure 3.35 two different realizations of metamutators, one CIM type and the other VIM type, are achieved.

By connecting ports y_1 and y_2 of FDCCII- in Figure 3.32 to ground and applying proper interconnections to other ports the metamutator in Figure 3.34 will be observed.

According to (3.14) the ports description matrix of metamutator will become as,

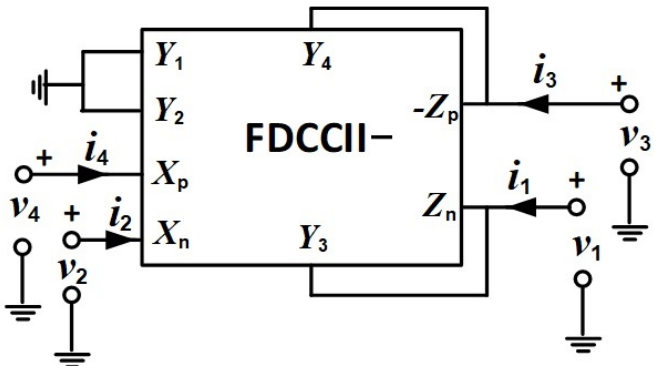


Figure 3.34: CIM type metamutator realized with single FDCCII-

$$\begin{bmatrix} i_1 \\ i_3 \\ v_2 \\ v_4 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_2 \\ -i_4 \\ v_3 \\ v_1 \end{bmatrix} \tag{3.15}$$

Comparing with (1.10) verifies the existence of CIM type configuration. In this case $n = 4, k = 1, l = 3$ and $m = 2$.

In Figure 3.32, by connecting the ports y_2, Z_p and Z_n of FDCCII- to ground and applying proper interconnections to other ports the metamutator in Figure 3.35 will be achieved.

According to (3.15) the ports description matrix of metamutator will become as,

$$\begin{bmatrix} i_1 \\ i_3 \\ v_2 \\ v_4 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_2 \\ i_4 \\ v_3 \\ -v_1 \end{bmatrix} \tag{3.16}$$

Comparing with (1.9) verifies the existence of VIM type metamutator configuration. In this case $n = 4, k = 1, l = 3$ and $m = 2$.

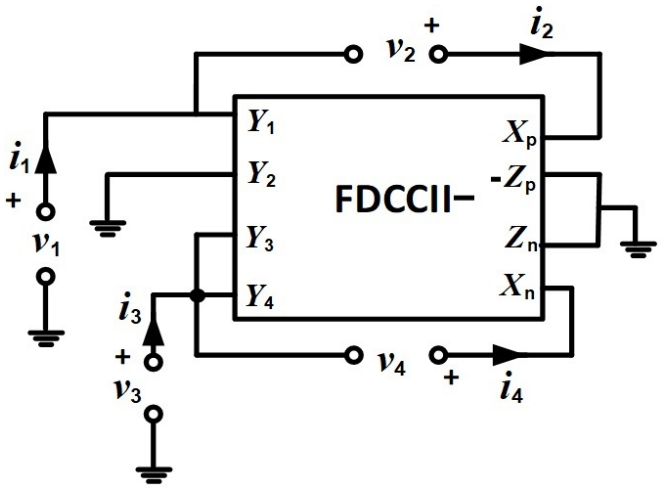


Figure 3.35: VIM type metamutator realized with single FDCCII-

As the ports description matrix of these newly proposed metamutators are the same as (1.9) and (1.10), the Table 1.3 stands true for these two metamutators.

In the sequel, frequency ranges in which metamutator realized with single FDCCII- shown in Figure 3.34 operates properly have been investigated. For FDCCII- TSMC, 0.18μA CMOS process parameters were used with transistor dimensions as shown in Table 3.4 and its circuit in Figure 3.5 (a) and Supply voltages are chosen as $\pm$0.9V, $V_{bp} = V_{bn} = 0$V and $I_B = I_{SB} = 50\mu$A.

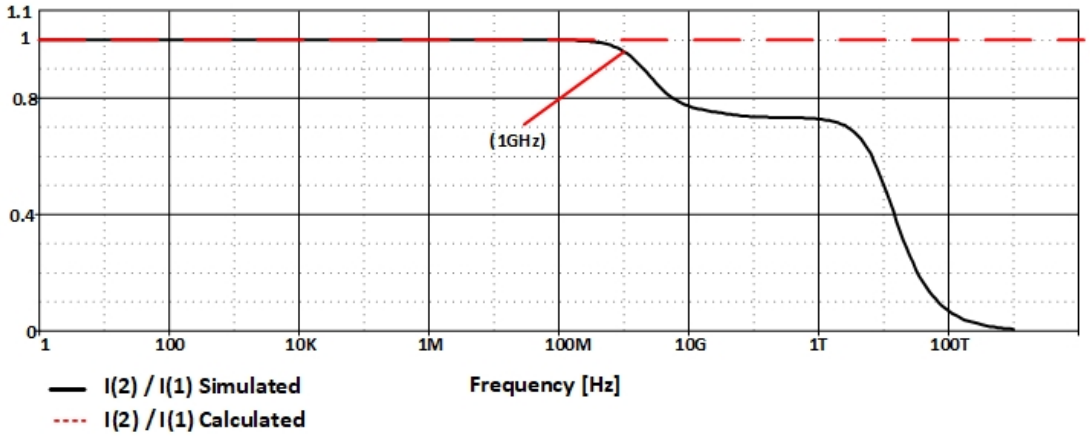


Figure 3.36: Ideal and non-ideal gain of i_1 and i_2

The characteristic in Figure 3.36 is achieved by applying an AC current source with amplitude of 100μA to port 1 and replacing 1Ω resistors in the other ports of FDCCII- based metamutator.

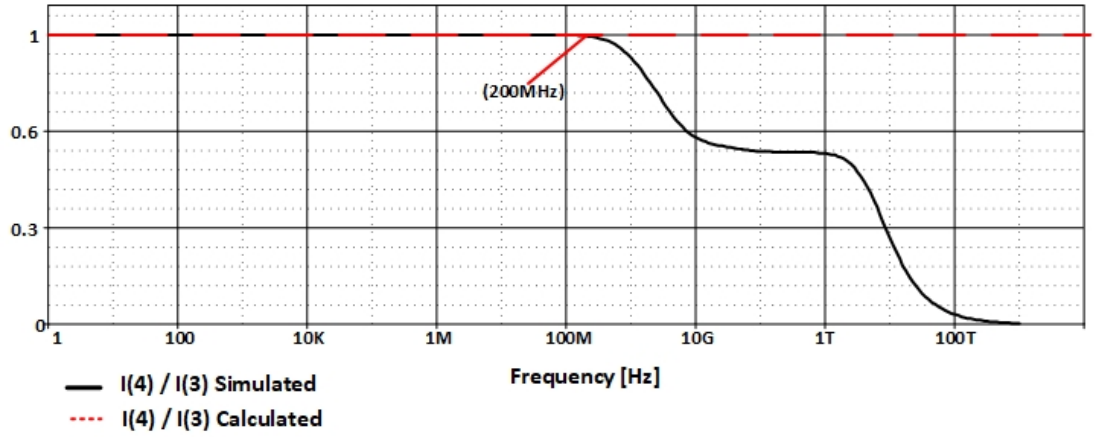


Figure 3.37: Ideal and non-ideal gain of i_2 and i_3

The characteristic in Figure 3.37 is achieved by applying an AC current source with amplitude of 100μA to port 3 and replacing 1Ω resistors in the other ports of FDCCII- based metamutator.

According to Simulation results in Figure 3.36 and Figure 3.37, currents match up until 1GHz and 200MHz respectively which prove the operation of FDCCII-based metamutator in a wide range of frequency as desired.

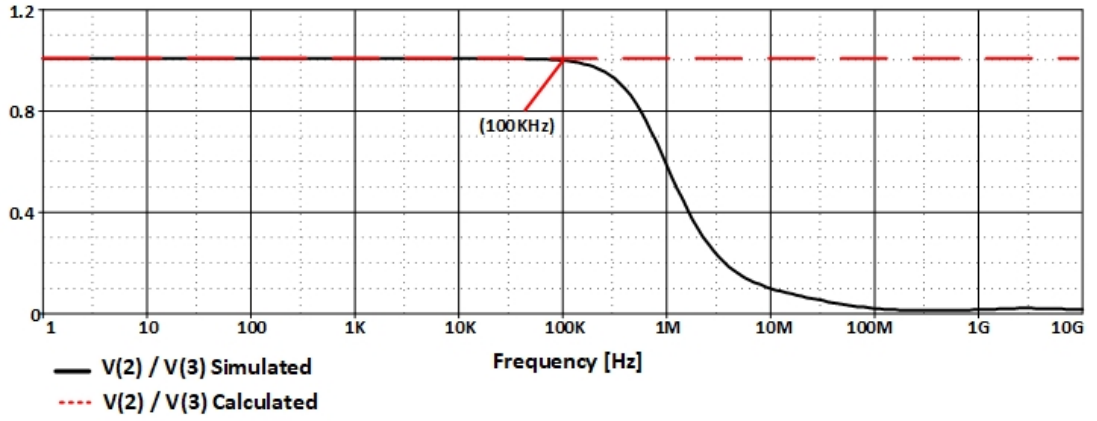


Figure 3.38: Ideal and non-ideal gain of v_2 and v_3

The characteristic in Figure 3.38 is achieved by applying an AC voltage source with amplitude of 1V to port 3 and replacing 100kΩ resistors in the other ports of FDCCII- based metamutator.

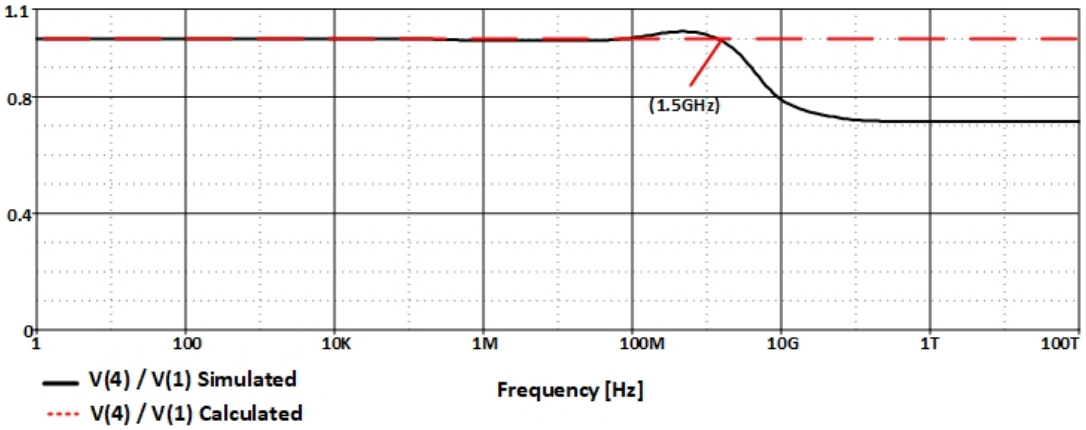


Figure 3.39: Ideal and non-ideal gain of v_4 and v_1

The characteristic in Figure 3.39 is achieved by applying an AC voltae source with amplitude of 1V to port 1 and replacing 100kΩ resistors in the other ports of FDCCII- based metamutator.

According to Simulation results in Figure 3.38 and Figure 3.39, currents match up until 100kHz and 1.5GHz respectively which prove the operation of FDCCII-based metamutator in a wide range of frequency as desired.

3.3.2 Realization with Dual X Current Conveyor (DXCCII)

Another newly proposed metamutator configuration employs only one Dual X Current Conveyor (DXCCII) which has 6 terminals including ground. By properly interconnecting the terminals of DCCII a metamutator will be obtained without usage of any other external elements.

The schematic block diagram of active element DCCII is shown in Figure 3.40

The port description matrix of DCCII is,

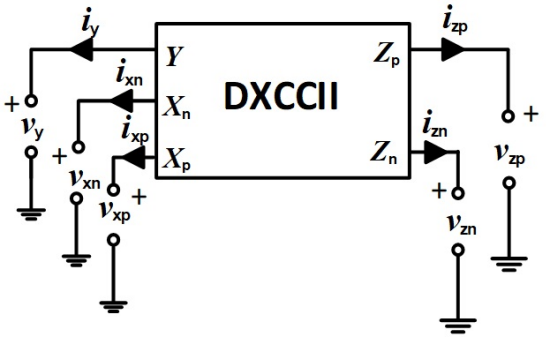


Figure 3.40: Schematic block diagram of DXCCII

$$\begin{bmatrix} v_{xp} \\ v_{xn} \\ i_{zp} \\ i_{zn} \\ i_y \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & 1 & -1 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 \end{bmatrix} \times \begin{bmatrix} v_y \\ i_{xp} \\ i_{xn} \\ v_{zp} \\ v_{zn} \end{bmatrix} \tag{3.17}$$

The CMOS realization of DXCCII extracted from [83] are shown below.

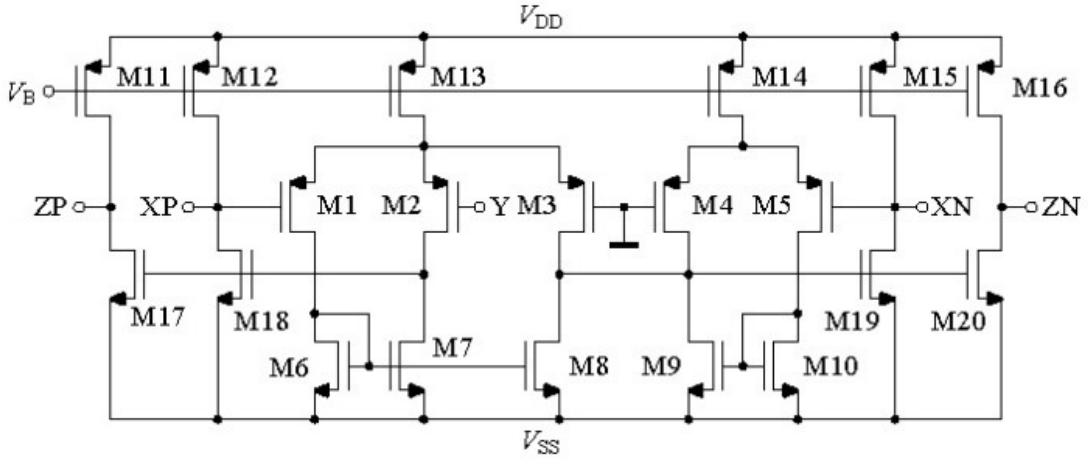


Figure 3.41: CMOS realization of DXCCII

Transistor dimensions are shown in Table 3.5.

By applying proper interconnections between the ports of DXCCII the metamutator configuration in Figure 3.42 will be achieved.

MOSFET	W (μm)	L (μm)
M_1, M_2,M_4, M_5, M_6, M_7, M_8, M_9, M_{10}, M_{17}, M_{18}, M_{19}, M_{20}	20	1.05
M_3	40	1.05
M_{11}, M_{12},M_{13}, M_{14}, M_{15}, M_{16}	50	1.05

TABLE 3.5: Dimension of transistors used in DXCCII

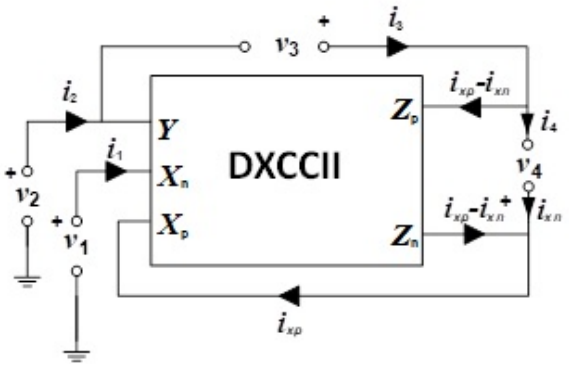


Figure 3.42: Newly proposed metamutator with DXCCII

According to (3.17) the ports description matrix of metamutator in Figure 3.42 will become as,

$$\begin{bmatrix} i_1 \\ v_2 \\ i_3 \\ v_4 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_4 \\ v_1 \\ i_2 \\ -v_3 \end{bmatrix} \tag{3.18}$$

Comparing with (1.9) verifies the existance of VIM type metamutator so the Table 1.3 stands true for this metamutator. In this case $n = 4, k = 3, l = 1$ and $m = 2$.

In the following, the frequency ranges in which the DXCCII based metamutator's port relations in (3.18) are satisfied will be investigated. For DXCCII TSMC, 0.35 μm CMOS process parameters were used with transistor dimensions as shown in Table 3.5 and its circuit in Figure 3.41, supply voltages are chosen as $\pm$1.65V, and V_B as 0.7V.

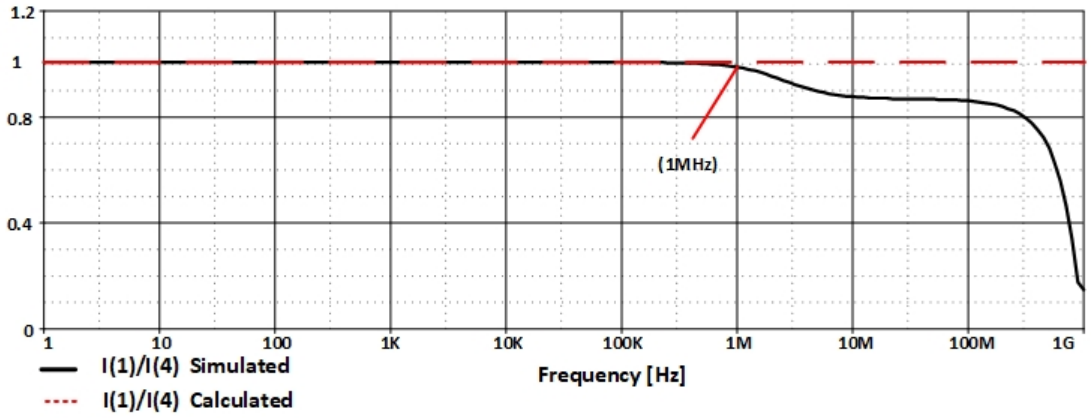


Figure 3.43: Ideal and non-ideal gain of i_1 and i_4

The characteristic in Figure 3.43 is achieved by applying an AC current source with amplitude of 100μA to port 4 and replacing 1Ω resistors in the other ports of DXCCII based metamutator.

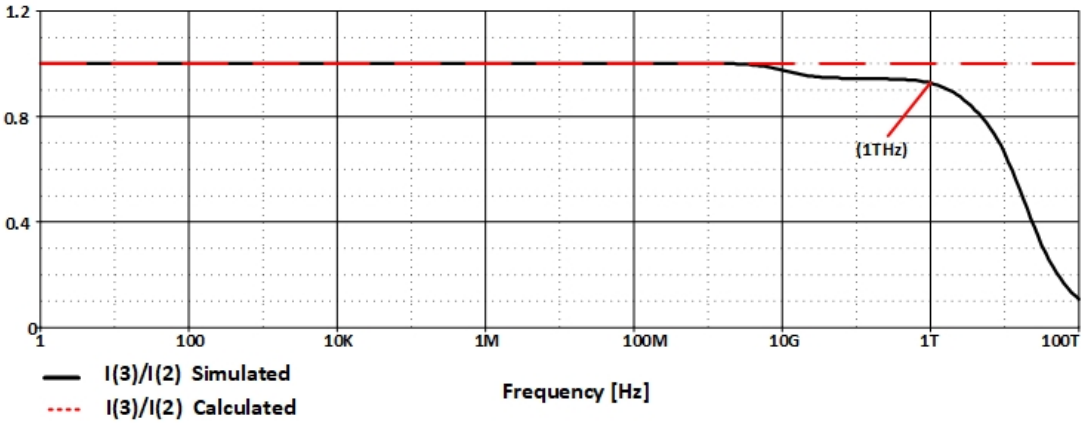


Figure 3.44: Ideal and non-ideal gain of i_3 and i_2

The characteristic in Figure 3.44 is achieved by applying an AC current source with amplitude of 100μA to port 2 and replacing 1Ω resistors in the other ports of DXCCII based metamutator.

According to Simulation results in Figure 3.43 and Figure 3.44, currents match up until 1MHz and 1THz respectively which prove the operation of DXCCII based metamutator in a wide range of frequency as desired.

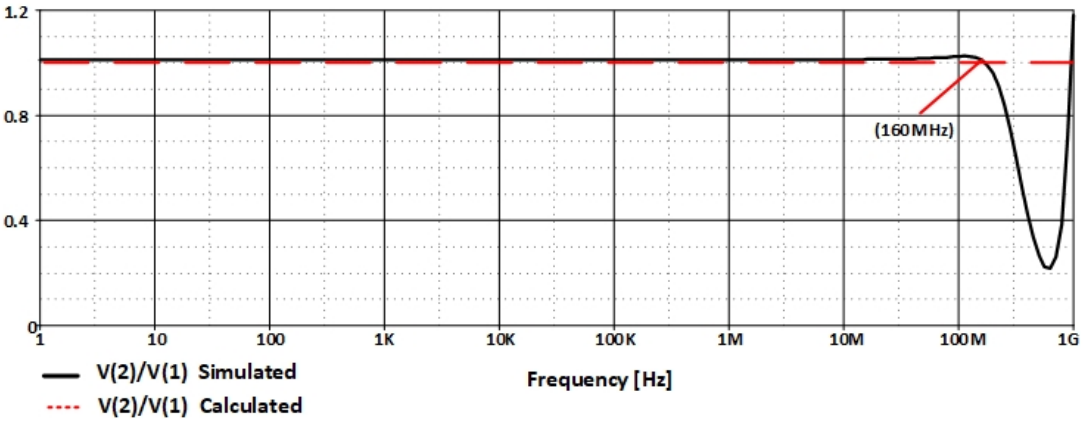


Figure 3.45: Ideal and non-ideal gain of v_2 and v_1

The characteristic in Figure 3.45 is achieved by applying an AC voltage source with amplitude of 1V to port 1 and replacing 100kΩ resistors in the other ports of DXCCII based metamutator.

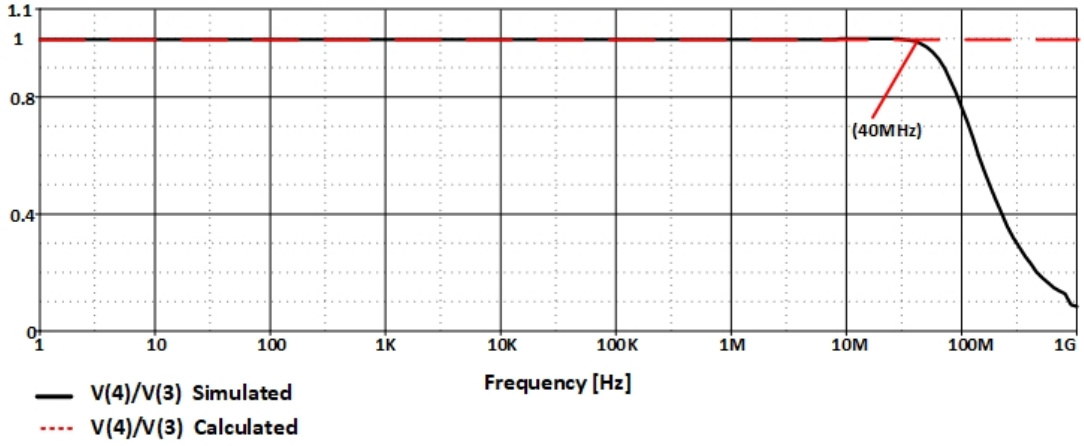


Figure 3.46: Ideal and non-ideal gain of v_4 and v_3

The characteristic in Figure 3.46 is achieved by applying an AC voltage source with amplitude of 1V to port 3 and replacing 100kΩ resistors in the other ports of DXCCII based metamutator.

According to Simulation results in Figure 3.45 and Figure 3.46 voltages match up until 160MHz and 40MHz respectively which prove the operation of DXCCII based metamutator in a wide range of frequency as desired.

3.3.3 Realization with Newly Designed AD-IC

The block diagram of newly designed Additive and Differential Integrated Circuit (AD-IC), built only with twelve transistors which has 5 terminals including ground. The schematic block diagram and ports description matrix of AD-IC are shown in Figure 3.47 and (3.19) respectively.

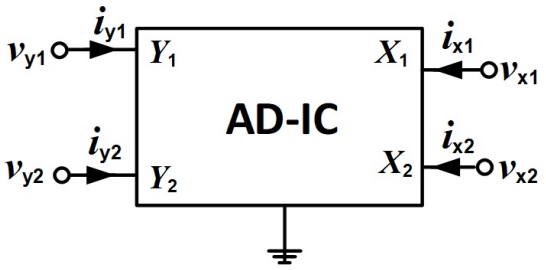


Figure 3.47: Schematic block diagram of AD-IC

$$\begin{bmatrix} v_{x1} \\ v_{x2} \\ i_{y1} \\ i_{y2} \end{bmatrix} = \begin{bmatrix} 1 & -1 & 0 & 0 \\ 1 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \times \begin{bmatrix} v_{y1} \\ v_{y2} \\ i_{x1} \\ i_{x2} \end{bmatrix} \tag{3.19}$$

In the realization of AD-IC, TSMC 0.25μm CMOS process parameters are used, with transistor dimensions as shown in Table 3.6 and its circuit structure in Figure 3.48.

MOSFET	W (μm)	L (μm)
M_1, M_2,M_5, M_6, M_7, M_8, M_9, M_{10}	1	0.5
M_{11}, M_{12},M_{13}, M_{14}	30	0.5

TABLE 3.6: Dimension of transistors used in AD-IC

The developed layout of the AD-IC circuit of Figure 3.48 is shown in Figure 3.49 The area of the AD-IC is calculated to be approximately 60X22μm^2.Post-layout simulations are performed with the parameters extracted from the layout netlist using TSMC 0.25μm process technology. The supply voltages are taken as $\pm$1.25V forV_{DD},V_{SS} and 0.8V for V_B.

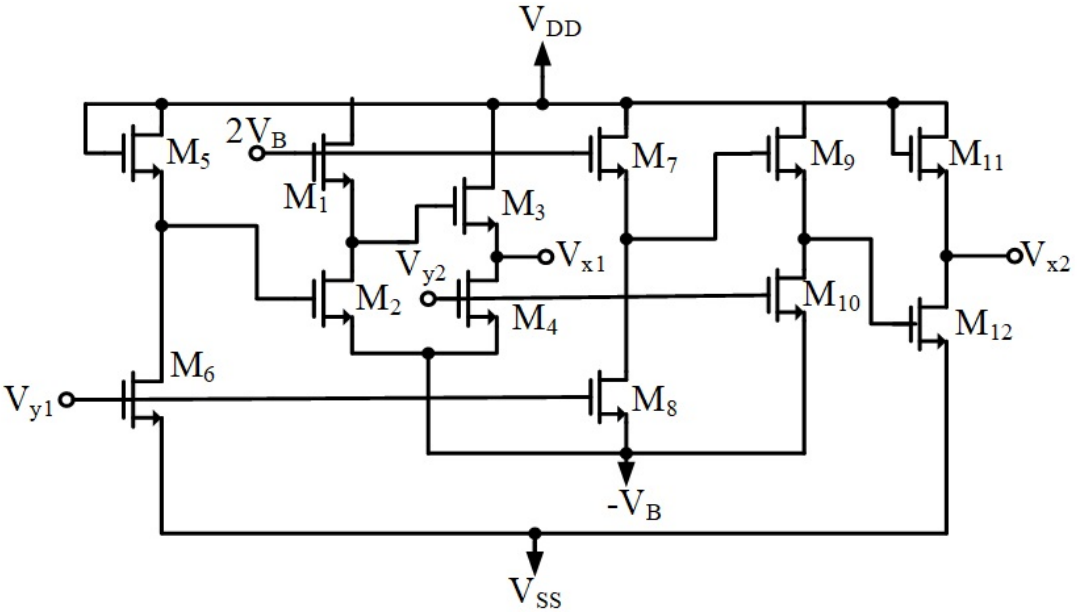


Figure 3.48: The implementation of AD-IC with twelve MOS transistors

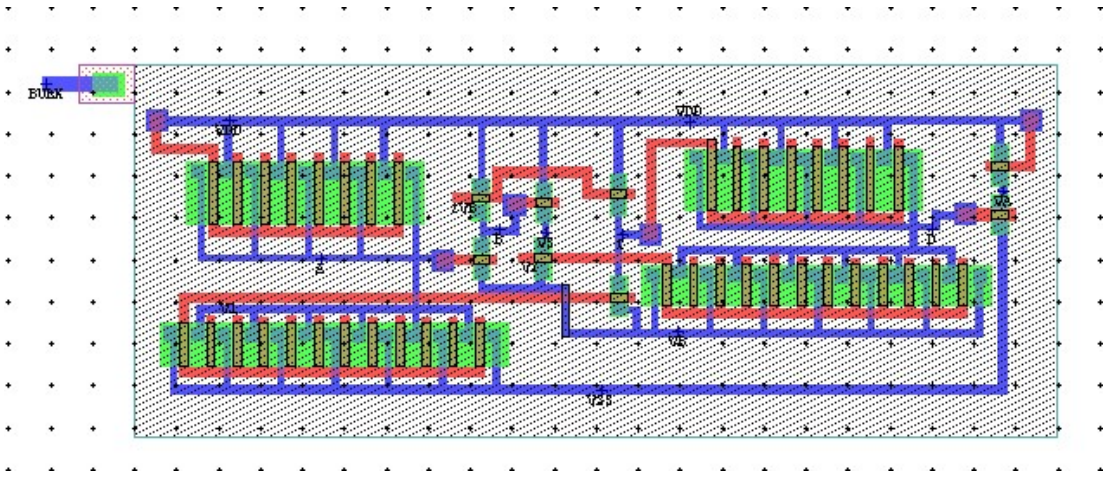


Figure 3.49: Layout of the AD-IC circuit

The equivalent parasitic capacitance C_L at the output terminal is approximately 73fF. The W/L ratios of the output node transistors M_3, M_4, M_{11} and M_{12} in Figure 3.48 are chosen much larger than the ratio of other transistors for the purpose of providing a smaller output resistance.

With proper interconnections of port branches as shown in Figure 3.50 a new realization of metamutators will be achieved.

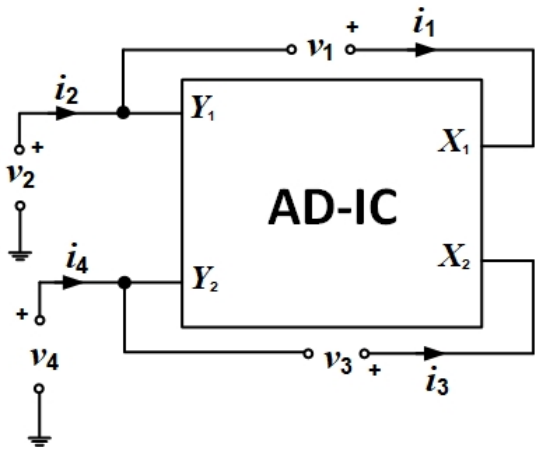


Figure 3.50: Schematic diagram of metamutator with AD-IC

According to (3.19) the ports description matrix of metamutator in Figure 3.50 will become as,

$$\begin{bmatrix} i_4 \\ i_2 \\ v_3 \\ v_1 \end{bmatrix} = \begin{bmatrix} 1 & 0 & 0 & 0 \\ 0 & 1 & 0 & 0 \\ 0 & 0 & 1 & 0 \\ 0 & 0 & 0 & 1 \end{bmatrix} \times \begin{bmatrix} i_3 \\ i_1 \\ v_2 \\ -v_4 \end{bmatrix} \tag{3.20}$$

Comparing with (1.9) verifies the existance of VIM type configuration so the Table 1.3 stands true for this metamutator. In this case $n = 1, k = 4, l = 2$ and $m = 3$. In continue the frequency range in which the AD-IC based metamutator operates optimally is investigated.

The characteristic in Figure 3.51 is achieved by applying an AC current source with amplitude of 100μA to port 4 and replacing 1Ω resistors in the other ports of AD-IC based metamutator.

The characteristic in Figure 3.52 is achieved by applying an AC current source with amplitude of 100μA to port 2 and replacing 1Ω resistors in the other ports of AD-IC based metamutator.

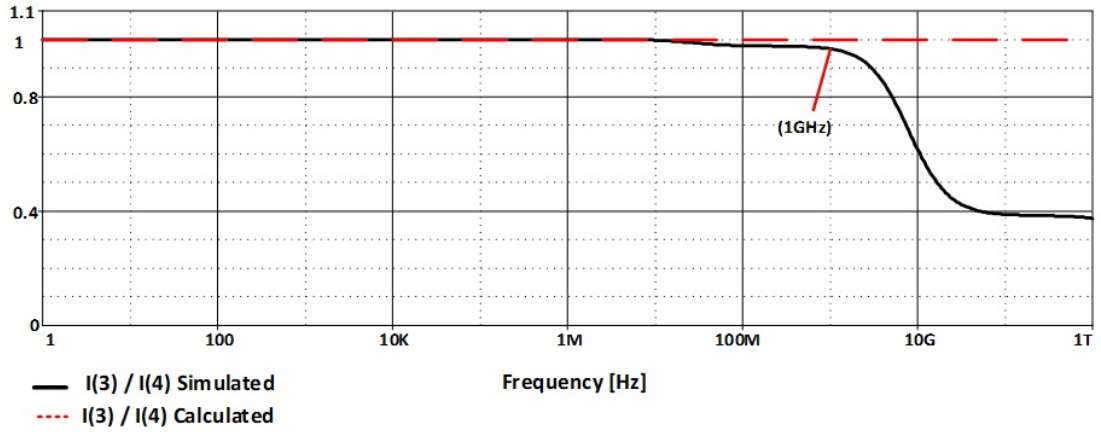


Figure 3.51: Ideal and non-ideal gain of i_3 and i_4

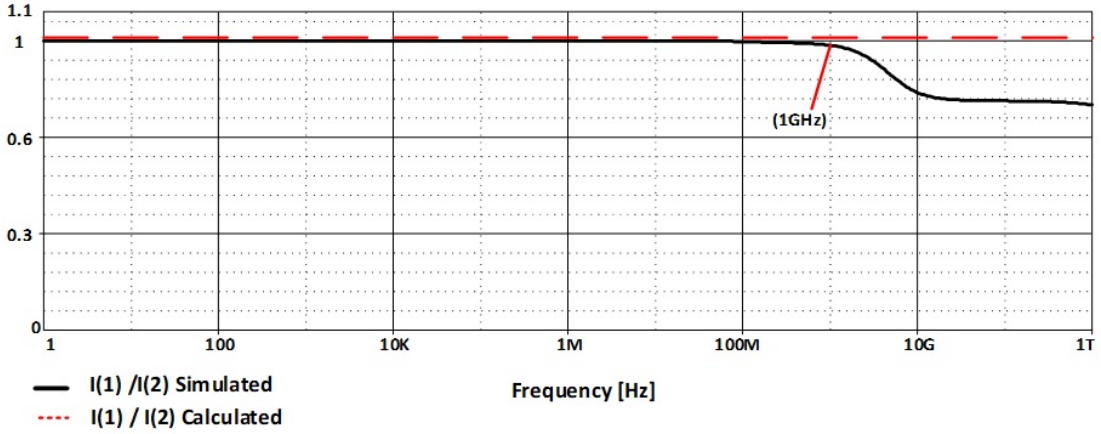


Figure 3.52: Ideal and non-ideal gain of i_1 and i_2

According to Simulation results in Figure 3.51 and Figure 3.52, currents match up until 5GHz in both of them which prove the operation of AD-IC based meta-mutator in a wide range of frequency as desired.

The characteristic in Figure 3.53 is achieved by applying an AC voltage source with amplitude of 1V to port 2 and replacing 100kΩ resistors in the other ports of AD-IC based metamutator.

The characteristic in Figure 3.54 is achieved by applying an AC voltage source with amplitude of 1V to port 4 and replacing 100kΩ resistors in the other ports of AD-IC based metamutator.

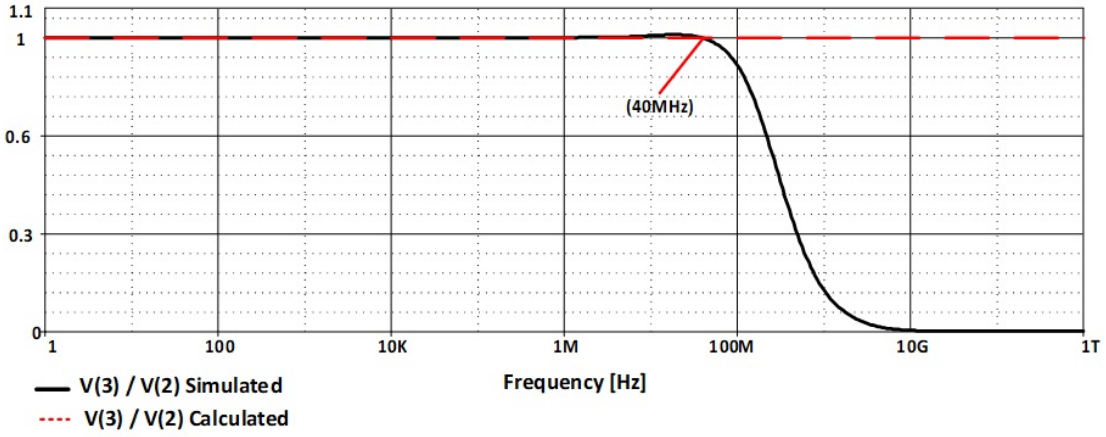


Figure 3.53: Ideal and non-ideal gain of v_3 and v_2

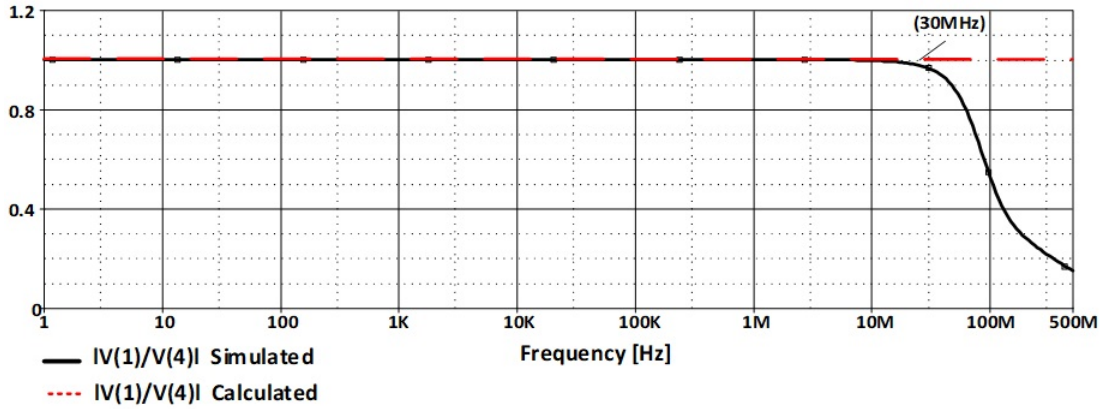


Figure 3.54: Ideal and non-ideal gain of v_4 and v_1

According to simulation results in Figure 3.53 and Figure 3.54, voltages match up until 40MHz and 30MHz which prove the operation of AD-IC based metamutator in a wide range of frequency as desired.

The frequency ranges in which incognito metamutators in the literature and the newly designed metamutators with Single Active Devices operate optimally are comparised and shown in Table 3.7.

Also a general comparison between all types of mutators is given in Table 3.8.

	Metamutator Realization	**Frequency Range for Optimal Current Ratio**	**Frequency Range for Optimal Voltage Ratio**	**# of Transistors**
In literature	CCII+, CCII-	100 MHz	30 MHz	32
	Adder/ Subtractor	2THz 1GHz	20MHz 100MHz	12
	CCII+, CF	80MHz 60MHz	20MHz	26
	2 CCII+	100MHz 30MHz	300MHz 70MHz	40
Here	FDCCII-	1GHZ 200MHz	100KHz 1.5GHz	32
	DXCCII	1MHz 1THz	160MHz 40MHz	20
	AD-IC	1GHZ	40MHz 30MHz	12

TABLE 3.7: Comparison between frequency range for optimal operation of incognito metamutators in literature and newly designed of metamutators

Ref.	# of active components	# of floating passive elements	# of grounded passive elements	Power supply	Floating/grou ndedmemrist or emulator	Sim/ Exp	# of Tra nsis tor
[100]	4 CCIIs (AD844) 1 multiplier (AD633)	2	4	±10V	Floating	Both	N*
[98]	2 OPAMP 1 Multiplier 10Transistor	1	2	±5V	Floating	Both	N
[102]	3 OTAs,4 CCIIs	3	4	±15V	Floating	Both	N
[99]	1 DDCC 1 Multiplier	-	2	±1.5V	Floating	Sim.	50
[101]	4 AD844s 1 OPAMP 1 Multiplier (AD633)	6	3	±15V	Floating	Both	N
[109]	10 DDCCs 8 Transistors	-	6	±1.25V	Grounded	Sim.	198
[107]	2 CCIIs (AD844) 1multiplier (AD633) 1 buffer (TL082)	1	3	±10V	Grounded	Both	N
[104]	2 CCIIs (AD844) 1 multiplier (AD633)	1	2	±10V	Grounded	Both	N
[105]	1 CCII (AD844) 1 multiplier (AD633)	1	1	±10V	Grounded	Both	N
[110]	3 CFOAs (AD844)	3	4	NA	Grounded	Exp.	N
[111]	2 CFOAs (AD844) 1 OTA (LM308)	-	5	±12V	Grounded	Exp.	N
[106]	1 MO-OTA 1 Multiplier	-	2	±1.25/±5V	Grounded	Both	38+
[42]	6 OTA (LM13600) Multiplier (AD633)	1	2	±10V	Floating	Both	N
[108]	CBTA Multiplier	1	2	±0.9	Grounded	Sim.	32+
Here	1 FDCCII -VIM	2	2	±0.9	Both	Sim.	32
Here	1 FDCCII-CIM	4	0	±0.9	Both	Sim.	32
Here	1 DXCCII	2	2	±1.65	Both	Sim.	20
Here	AD-IC	2	2	±1.25	Both	Sim.	12

*N: Not in transistor level

TABLE 3.8: General comparison between all types of mutators

Chapter 4

Different Applications of Metamutators

In this chapter, applications of metamutators developed during the research period of this thesis will be presented. As the port description matrix of all introduced metamutators in chapter 3 are the same as (1.9) for VIM type and (1.10) for CIM type metamutators, all of the applications in this chapter stand true for all of metamutators. Depending on how some of the ports are terminated, many metamutator applications, which can be classified in two groups, will be attained:

I. 1-port circuits realized with metamutators,

II. 2-port circuits realized with metamutators.

In 1-port realizations, by properly terminating three ports of the metamutator the resulting circuit will behave as the desired 2-terminal element at the fourth port. A list of so realizable 2-terminal elements is depicted with Table 1.3.

In 2-port realizations, by properly terminating two metamutator ports the resulting circuit will behave as the desired 2-port from the remaining two ports. A list of so realizable 2-ports is given with Table 4.5.

These applications will be examined in detail with PSPICE simulations using transistor parameters obtained from layout level descriptions of metamutators and comparison between simulation results and theoretical results will be demonstrated in sections 4.1 and 4.2 realizations of 1-Port.

4.1 Realization of 1-ports

4.1.1 Mutating Nonlinear Resistor to Memristor

To illustrate the working principle of the metamutator as a memristor mutator, the realization in row #12 of Table 1.3 has been applied to the metamutator with AD-IC. By terminating ports 3, 4 and 2 of the metamutator in Figure 3.50 with a nonlinear resistor, inductor and capacitor respectively a memristor is obtained at port 1. The circuit structure is shown in Figure 4.1.

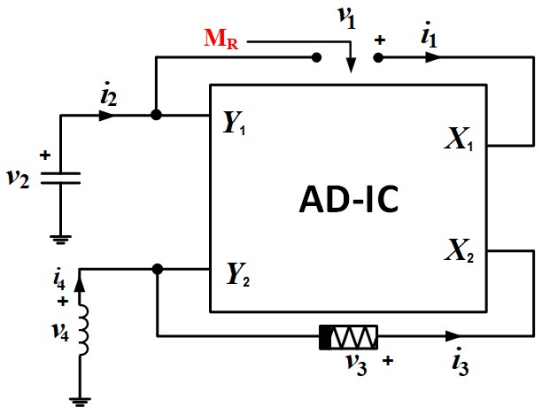


Figure 4.1: Memristor realization with AD-IC based metamutator

The nonlinear-resistor modeled by the circuit presented in [26] and shown in Figure 4.2 is used.

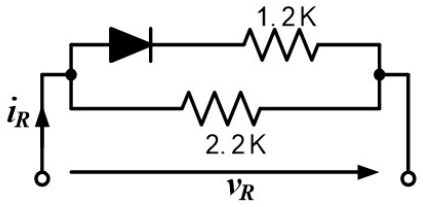


Figure 4.2: Implementation on non-linear load of M-R mutators.

The port analysis of this circuit is as follow. Let the definition of the nonlinear-resistor at port 3, with the assigned polarities, be given by (4.1),

$$f(i_3, -v_3) = 0 \tag{4.1}$$

Replacing i_3 with i_4 and v_3 with v_2 according to (3.20), gives:

$$f(i_4, -v_2) = 0 \tag{4.2}$$

Use of the elements' constitutive relations $i_4 = -\varphi_4/L$ and $-v_2 = q_2/C$ in (1.10) results in,

$$f(\frac{-\varphi_4}{L}, \frac{q_2}{C}) = 0 \tag{4.3}$$

Finally, use of (3.20) again to replace φ_4 and q_2 by $-\varphi_1$ and q_1 respectively, yields (4.4) which is a memristor constitutive relation with the same characteristic, within scaling factors L and C, as the nonlinear resistor in Figure 4.1. In order for expression (4.4) to conform with expression (4.1) the polarities of the memristor so obtained should have the same relative position.

$$f(\frac{\varphi_1}{L}, \frac{q_1}{C}) = 0 \tag{4.4}$$

By comparing (4.4) and (2.4), the scaling factors $K_x = C$ and $K_y = L$ can be verified.

Selecting a sinusoidal voltage source with amplitude 3.5V and frequency of 30 Hz at port 4 of the metamutator in Figure 4.1, the current versus voltage characteristic has been obtained as shown in Figure 4.3. For the nonlinear resistor the model shown in Figure 4.2 and for AD-IC TSMC, 0.25μm CMOS process parameters are used with transistor dimensions as shown in Table 3.6 and its circuit in Figure 3.48. Supply voltages are chosen as $\pm$1.25V, $V_B = 0.8$V. The capacitor and

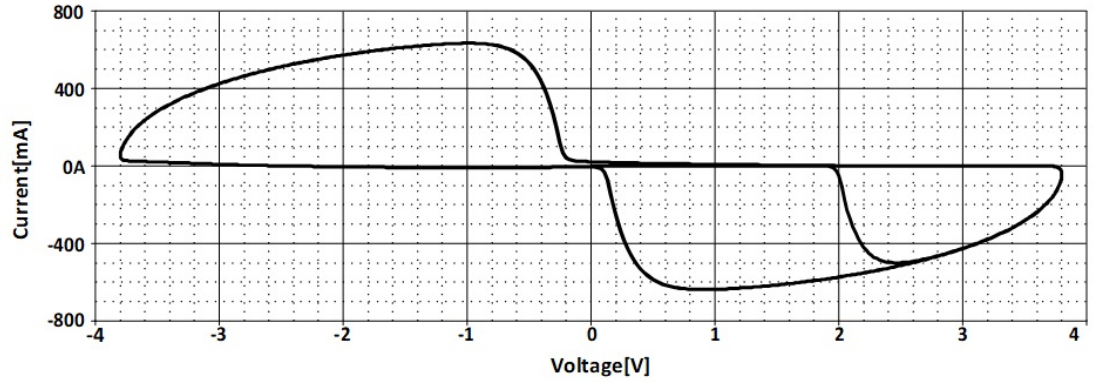


Figure 4.3: $i - v$ characteristic of memristor

inductor values were selected as 0.1nF and 2.5mH, respectively. The Lissajous curve in Figure 4.1 confirms the signature of a memristor at port 4.

4.1.2 Mutating Memristor to Meminductor

To illustrate the working principle of the metamutator as meminductor mutator, the metamutator structure in Figure 3.10 is chosen. By terminating ports 2, 3, 4 of the metamutator with capacitor, memristor and resistor respectively, according to row #4 of Table 1.3, the circuit in Figure 3.10 becomes as shown in Figure 4.4 and a meminductor results at port 1.

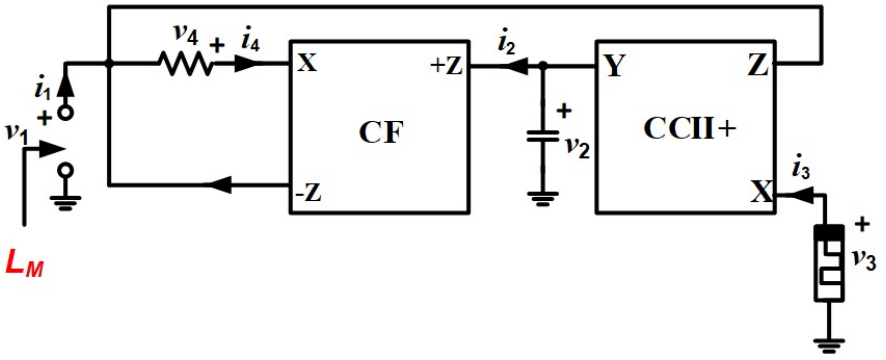


Figure 4.4: Meminductor realization with memristor terminated metamutator

The port analysis of this circuit is as follows: the definition of memristor at port 3 is,

$$f(q_3, -\varphi_3) = 0 \tag{4.5}$$

Replacing q_3 and φ_3 by q_1 and φ_2 respectively according to (3.5) gives,

$$f(q_1, -\varphi_2) = 0 \tag{4.6}$$

Using the element constitutive relation $v_2 = -q_2/C$ at port 2 then taking the integral of both hand sides gives $\varphi_2 = -\sigma_2/C$ and replacing σ_2 by σ_4 to (4.6) gives,

$$f(q_1, \frac{\sigma_4}{C}) = 0 \tag{4.7}$$

Finally, as $v_4 = -R.i_4$ implies $\rho_4 = -R.\sigma_4$ and $\sigma_4 = -\rho_4/R$ Replacing ρ_4 by $-\rho_1$, yields the meminductor's constitutive relation shown with (4.8),

$$f(q_1, \frac{\rho_1}{RC}) = 0 \tag{4.8}$$

By comparing (4.8) and (2.16) the scaling factors $K_x = RC$ and $K_y = 1$ can be deduced. The PSPICE simulation result given in Figure 4.5 confirms very well the signature of a meminductor.

The circuit in Figure 4.4 is simulated by placing a sinusoidal current source to port 1 with amplitude and frequency of 10mA and 20Hz. For the memristor, the HP model with parameter values of $\mu_v = 10^{(-10)}.cm^2.s^{(-1)}.v^{(-1)}$, R_{on}=10Ω, R_{off}=20kΩ, R_{init}=5kΩ, and as window function the Joglekar's model [28] $f(x) = 1–(2x–1)^{2p}$ with p=10, for CF and CCII+, 0.13μm CMOS technology parameters have been used. The transistor level circuits are shown in Figure 3.5 and Figure 3.12, parameters being given in Table 3.1 and Table 3.3 respectively; supply

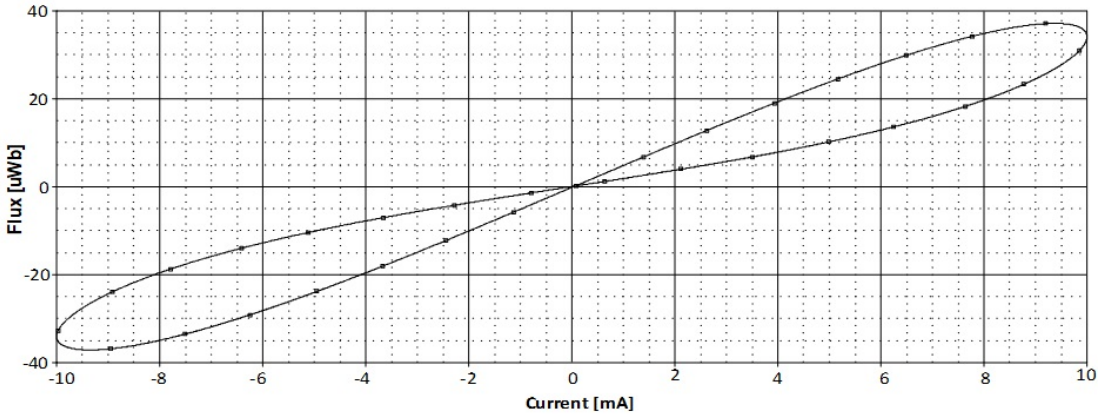


Figure 4.5: $\varphi - i$ characteristic of meminductor

voltages are selected as ± 0.75V, $V_B = 0.24$V and resistor and capacitor values as 1kΩ and 1nF, respectively.

4.1.3 Mutating Memristor to Memcapacitor

To illustrate the working principle of the metamutator, as memcapacitor mutator , according to realization in row #5 of Table 1.3, ports 2, 3 and 4 of the metamutator in Figure 3.2 are terminated with memristor, inductor and resistor respectively. The circuit becomes as shown in Figure 4.6 and a memcapacitor is obtained at port 1.

The port analysis of this circuit is as follows. The definition of memristor at port 2 is:

$$f(q_2, -\varphi_2) = 0 \tag{4.9}$$

According to (3.3) replacing q_2 and φ_2 with q_3 and φ_1 respectively gives,

$$f(q_3, -\varphi_1) = 0 \tag{4.10}$$

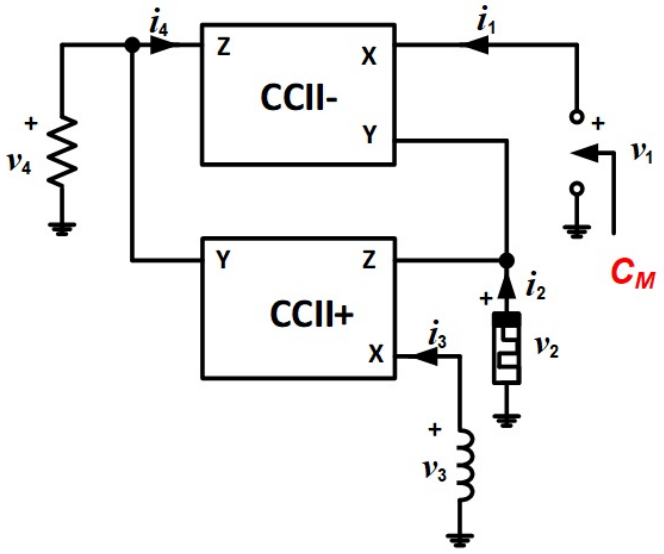


Figure 4.6: Memcapacitor realization with memristor terminated metamutator

Use of the elements' of constitutive relations $q_3 = -\rho_3/L$ and $\rho_3 = \rho_4 = -R.\sigma_4$ so $q_3 = R.\sigma_4/L$ as $\sigma_4 = -\sigma_1$ yields the memcapacitor's constitutive relation in (4.11).

$$f((R/L).\sigma_1, \varphi_1) = 0 \tag{4.11}$$

By comparing (4.11) and (2.19), the scaling factors$K_x = L/R$ and $K_y = 1$ are observed. The PSPICE simulation result in Figure 4.7 confirms very well the signature of a memcapacitor.

Circuit in Figure 4.7 is simulated by applying a sinusoidal voltage source to port 1 with an amplitude and frequency of 2V and 50Hz respectively. As memristor the HP model with parameters R_{on}=1kΩ, R_{off}=100kΩ, R_{init}=10kΩ, $\mu_v = 10^{(-10)}.cm^2.s^{(-1)}.v^{(-1)}$ and as window function, Joglekar's model [28] $f(x) = 1–(2x–1)^{2p}$ with p=10 are used. As CCII+ and CCII- the CMOS realizations with the same transistor parameters introduced in Chapter 3.1.1 were used. The resistor and capacitor values were selected as 1kΩ and 10nF, respectively.

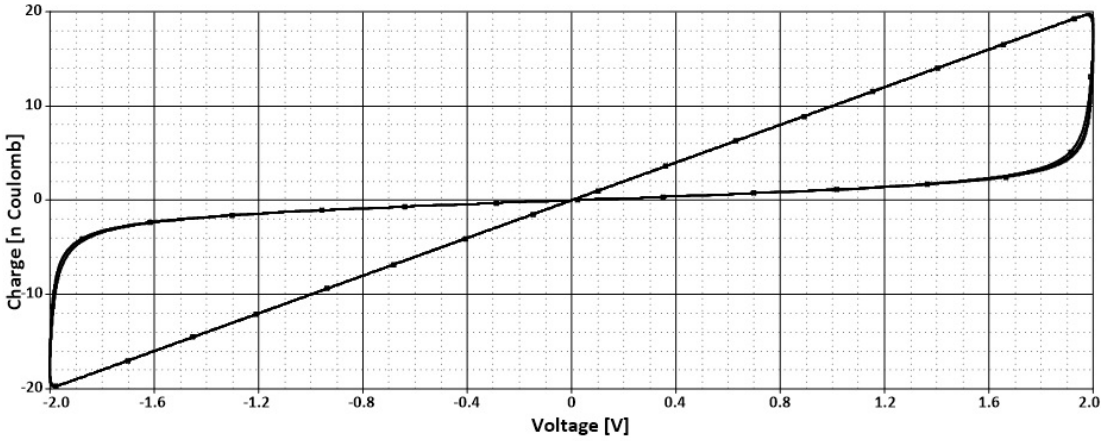


Figure 4.7: $q - v$ characteristic of the memcapacitor

4.1.4 Floating and Grounded Impedance Scaling

In this section floating and grounded impedance scaling applications of the new AD-IC based metamutator will be presented. By connecting impedances to three of the ports, the impedance as seen from the remaining fourth port can be found in terms of the connected ones as shown in Table 4.1. When reading column i of Table 4.1 it should be understood that no element is connected to port i whereas impedances Z_j are connected to port$j$ for $j \neq i$ and $i = n, l, m, k$.

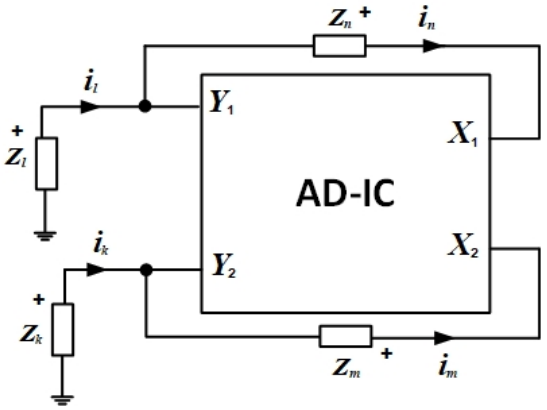


Figure 4.8: Metamutator terminated with port impedances

As an example assume $i = n$, in this case the other three ports are terminated with Z_l, Z_m and Z_k as illustrated in Figure 4.9.

	Port$n$	**Port**l	**Port**m	**Port**k
Type	Floating	Grounded	Floating	Grounded
Z	$Z_n = \frac{Z_k}{Z_m}.Z_l$	$Z_l = \frac{Z_m}{Z_k}.Z_n$	$Z_m = \frac{Z_l}{Z_n}.Z_k$	$Z_k = \frac{Z_n}{Z_m}.Z_l$

TABLE 4.1: Equivalent impedance at the ports

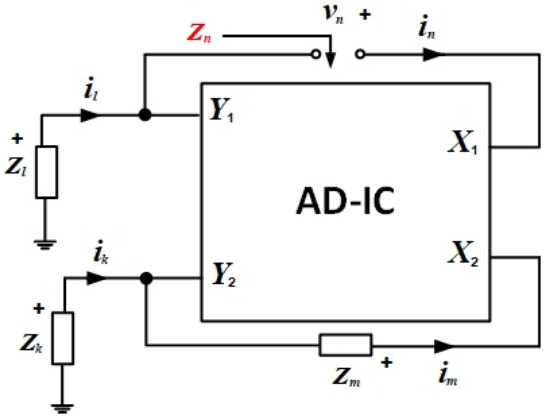


Figure 4.9: Port n of metamutator terminated with impedance Z_n

After some algebraic manipulations using KCL and KVL and the port relation matrix described in (3.20) , the impedance at the fourth port will be obtained as in (4.12).

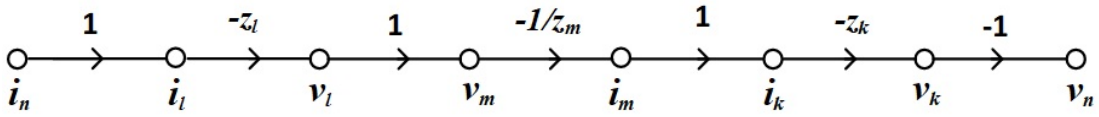


Figure 4.10: Impedance scaling calculated with signal flow-graph

$$v_n = (-Z_l).\frac{-1}{Z_m}.(-Z_k).(-1).i_n \rightarrow Z_n = \frac{v_n}{i_n} \rightarrow Z_n = \frac{Z_k.Z_L}{Z_m} \tag{4.12}$$

An interesting conclusion that can be deduced from Table 4.1 is that the metamutator allows the realization of grounded elements as well as floating ones.

4.1.4.1 Inductance Simulator

As coil realization of inductors on an integrated chip is highly undesirable many inductor simulators have been proposed in the literature [29-30]. In this section an application of metamutators as inductance simulator with a minimum number of elements, only one active device AD-IC with 12 transistors, two resistors and single capacitor, will be presented. According to Table 4.1 by properly connecting one capacitor and two resistors to three of the ports, an inductor will result at the fourth port. In this case the inductance value is equal to the product of the values of capacitor and resistors. Four different realizations are shown in Table 4.2.

Realization	**Port**n	**Port**l	**Port**m	**Port**k	Inductance
#1	L_{eq}	R_l	C_m	R_k	$L_{eq} = C_m R_l R_k$
#2	R_n	L_{eq}	R_m	C_k	$L_{eq} = C_k R_n R_m$
#3	C_n	R_l	L_{eq}	R_k	$L_{eq} = C_n R_l R_k$
#4	R_n	C_l	R_m	L_{eq}	$L_{eq} = C_l R_m R_n$

TABLE 4.2: Different realizations of inductor

To demonstrate an example, realization #2 of Table 4.2 will be considered. By connecting C_k, R_n and R_m to three of the ports of the metamutator with AD-IC, an inductor will be obtained at port l:

$$Z_l = \frac{Z_m.Z_k}{Z_n} = \frac{R_m}{\frac{1}{sC_k}}.R_n = sC_k R_m R_n \rightarrow L_m = C_k R_m R_n \tag{4.13}$$

Equality (4.13) clearly confirms the existence of inductor at port l. Furthermore, the performance of the proposed inductance is verified with the frequency response plots of the actual and ideal inductor both given in Figure 4.11.

In this case the metamutator was simulated using an AC current source with amplitude of 1mA. For AD-IC the CMOS realization with the same transistor parameters introduced in subsection 3.3.3 was used. The values of resistors and

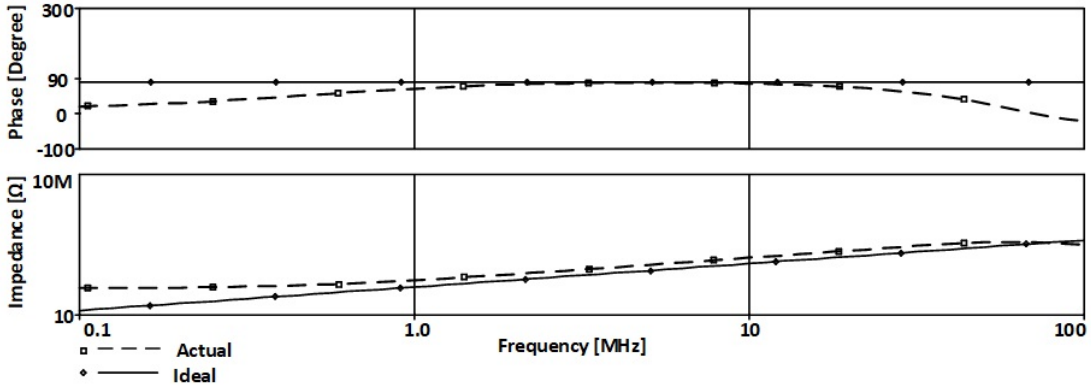


Figure 4.11: Phase and |impedance| plots of the inductor vs. frequency

capacitors have been selected as $R_n = R_m = 1$ kΩ and $C_k = 25$pF, which correspond to an inductance of 25μH.

4.1.4.2 Capacitance Multiplier

In the design of integrated circuits, Capacitance Multipliers are being used for the realization of large-valued capacitances on chip. The capacitance multiplier can save valuable space on the chip in exchange for use of one active element and two/three passive components. The final multiplied capacitance is larger than one real on-chip capacitance, with smaller on-chip space required. In this section an application of metamutator as capacitance multiplier, with minimum number of elements and only one active device AD-IC with 12 transistors, is presented. According to Table 4.1 by properly connecting one capacitor and two resistors to three of the ports, a capacitor will be obtained at the fourth port. The different realizations are shown in Table 4.3.

Applying realization in row #3 of the Table 4.3 to the metamutator with AD-IC by connecting C_m, R_n and R_k to three of the ports of metamutator, a capacitor with capacitance value of $K.C_m$ will be obtained at port l. In this case K is the ratio of resistors in the other two ports.

Realization	**Port**n	**Port**l	**Port**m	**Port**k	Capacitance
#1	C_{eq}	C_l	R_m	R_k	$C_{eq} = \frac{C_l.R_m}{R_k}$
#2	C_{eq}	R_l	R_m	C_k	$C_{eq} = \frac{C_k.R_m}{R_l}$
#3	R_n	C_{eq}	C_m	R_k	$C_{eq} = \frac{C_m.R_k}{R_n}$
#4	C_n	C_{eq}	R_m	R_k	$C_{eq} = \frac{C_n.R_k}{R_m}$
#5	R_n	C_l	C_{eq}	R_k	$C_{eq} = \frac{C_l.R_n}{R_k}$
#6	R_n	R_l	C_{eq}	D_k	$C_{eq} = \frac{C_k.R_n}{R_l}$
#7	C_n	R_l	R_m	C_{eq}	$C_{eq} = \frac{C_n.R_l}{R_m}$
#8	R_n	R_l	C_m	C_{eq}	$C_{eq} = \frac{C_m.R_l}{R_n}$

TABLE 4.3: Capacitance multiplier realizations

$$Z_l = \frac{Z_m.Z_k}{Z_n} = \frac{\frac{1}{sC_m}}{R_k}.R_n \Rightarrow C_l = C_m\frac{R_k}{R_n} \tag{4.14}$$

Equality (4.14) clearly confirms the existence of a capacitor in port l for which the capacitance value is $C_m.R_k/R_n$. Moreover, the frequency response plots of the multiplied capacitor and that of an ideal capacitor are given with Figure 4.12.

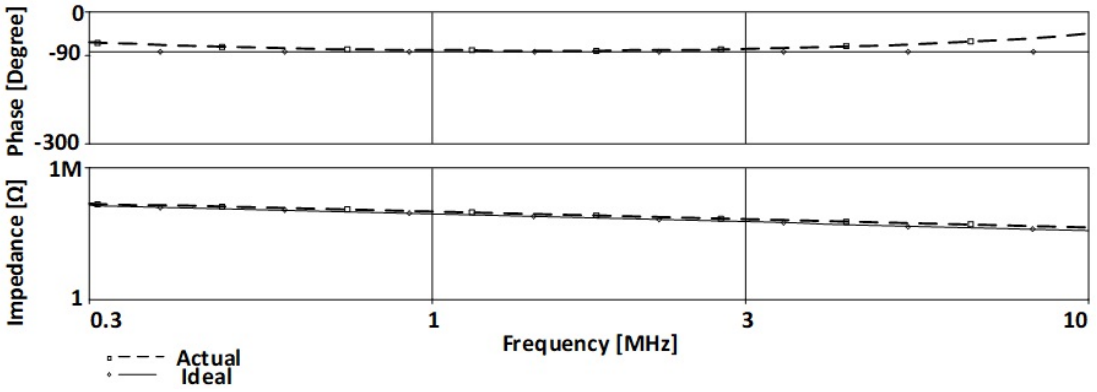


Figure 4.12: Phase and |impedance| plots of the capacitor vs. frequency

In this case the metamutator was simulated using an AC voltage source with amplitude of 0.3V; For AD-IC the CMOS realization with the same transistor parameters introduced in chapter 3.3.3 were used. The values of resistors and capacitors have been selected as R_n= 1kΩ, R_k= 20kΩ and C_m= 5pF, which corresponds to the value of multiplied capacitance of 100pF.

4.1.4.3 Frequency Dependent Negative Resistor Simulator

Low-pass filters have wide usage in radio frequency (RF) transceivers; in this process the frequently used low-pass filter is called Anti-Aliasing Filter (AAF). By reducing the size and refining the performance of these filters, new improvements in communication are achieved. Figure 4.13 shows the position of AAF in fully digital receivers.

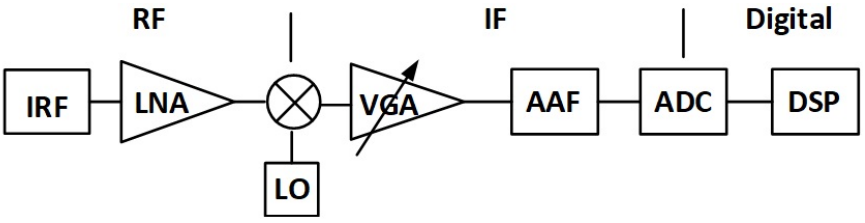


Figure 4.13: Schematic of fully digital receiver [31]

As in general AAF are third or higher order passive LC ladder filters, using an inductor in these circuits requires a lot of space and reduces the performance. In order to decrease the size and improve the performance one can use the complex impedance scaling technique for designing a prototype of the LC ladder circuits. This technique, treated extensively by Bruton [32], is based on the fact that the filter transfer function will remain unchanged if the impedance of each element is divided by "s". So the Inductor will be transformed into a resistor, the resistor will be transformed into a capacitor and a capacitor will be transformed into a Frequency Dependent Negative Resistor (FDNR).

By connecting two capacitors and one resistor to three of the ports, as detailed in Table 4.1, a grounded or floating FDNR will be observed from the fourth port. Different realizations and values of FDNRs are shown in Table 4.4.

It should be observed again that only twelve transistors and three passive elements are being used with no component matching requirements.

Realization	**Port**n	**Port**l	**Port**m	**Port**k	Capacitance
#1	D_{eq}	C_l	R_m	C_k	$D_{eq} = \frac{1}{s^2 C_l C_k R_m}$
#2	C_n	D_{eq}	C_m	R_k	$D_{eq} = \frac{1}{s^2 C_n C_m R_k}$
#3	R_n	C_l	D_{eq}	C_k	$D_{eq} = \frac{1}{s^2 C_l C_k R_n}$
#4	C_n	R_l	C_m	D_{eq}	$D_{eq} = \frac{1}{s^2 C_n C_m R_l}$

TABLE 4.4: FDNR realizations

Applying realization #4 to the metamutator with AD-IC as given in Table 4.4 and connecting C_n, R_l and C_m to ports n, l and m of the metamutator respectively, a FDNR will be observed from port k.

$$Z_k = \frac{Z_n.Z_l}{Z_m} = \frac{\frac{1}{sC_n}}{R_l}.\frac{1}{sC_m} = \frac{1}{s^2 C_m C_n R_L} \quad \Rightarrow \quad D_k = -\frac{1}{w^2 C_m C_n R_l} \tag{4.15}$$

Equality (4.15) clearly confirms the existence of FDNR in the fourth port. Moreover, the frequency domain phase and impedance characteristics of FDNR are given in Figure 4.14.

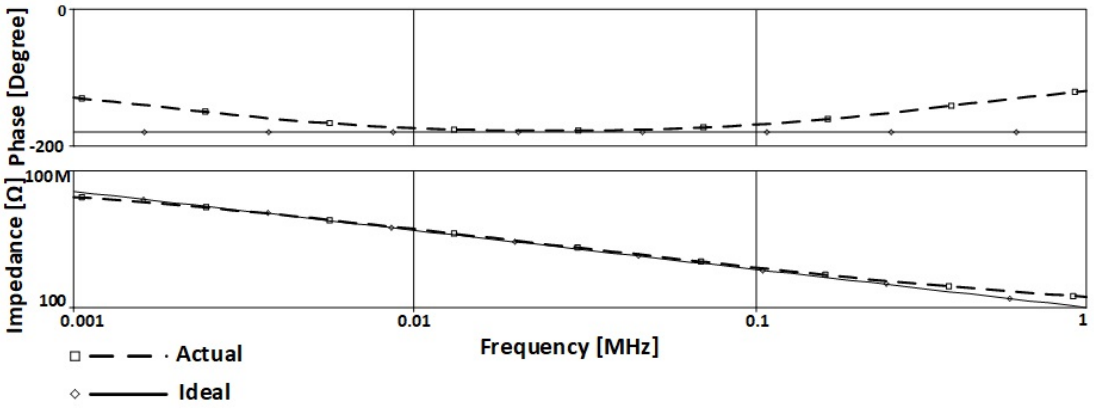


Figure 4.14: Characteristics of FDNR in frequency domain

The metamutator with AD-IC was simulated using an AC voltage source with amplitude of 1V. For AD-IC the CMOS realization with the same transistor parameters introduced in chapter 3.3.3 was used. The values of C_n, C_m and R_l were selected as 0.1nF, 0.2nF and 100kΩ, respectively.

4.1.5 RC-Oscillators

First quadrature feedback oscillator realization using metamutators was given in [120]. Another new application of metamutator is its application as RC-oscillator. The schematic block diagram of an RC oscillator is shown in Figure 4.15. By applying this realization and selecting port l as output port, one can prove the existence of an oscillator.

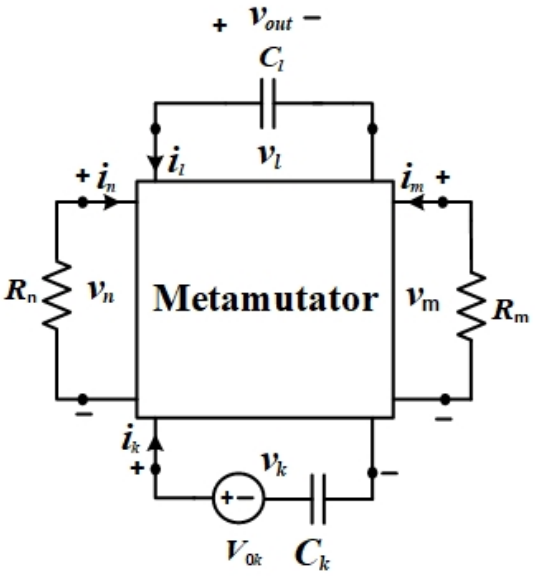


Figure 4.15: Block diagram of the RC-oscillator

Writing KVL and KCL the current at port$k$ is,

$$i_k = sC_k(V_{0k} - v_k) \tag{4.16}$$

and substituting circuit variables according to (3.20) gives,

$$i_k = sC_k(V_{0k} - v_k) = i_m = -\frac{v_m}{R_m} = -\frac{v_l}{R_m} \tag{4.17}$$

After some algebraic manipulations expression (4.17) becomes as given with:

$$sC_kV_{0k} + \frac{v_l}{R_m} = sC_kV_k \tag{4.18}$$

From the expression of the current for port l:

$$i_l = -sC_lV_l = i_n = -\frac{v_n}{R_n} = \frac{v_k}{R_n} \quad \Rightarrow \qquad sV_l = -\frac{v_k}{R_nC_l} \tag{4.19}$$

is obtained, so (4.18) and (4.19) together give,

$$\begin{bmatrix} sV_l \\ sV_k \end{bmatrix} = \begin{bmatrix} 0 & -\frac{1}{C_lR_n} \\ \frac{1}{C_kR_m} & 0 \end{bmatrix} \times \begin{bmatrix} V_l \\ V_k \end{bmatrix} + \begin{bmatrix} 0 \\ 1 \end{bmatrix} sV_{0k} \tag{4.20}$$

Calculation of the determinant of the state matrix gives imaginary eigenvalues:

$$det(sI - A) = s^2 + {w_0}^2 \qquad and \qquad {w_0}^2 = \frac{1}{C_lR_nC_kR_m} \tag{4.21}$$

It is well-known that the time-domain zero-input solution for $V_{out} = V_l(s)$ is of the form,

$$v_(out) = a_1e^{-jw_0t} + \overline{a_1}e^{-jw_0t} = 2|a_1|cos(w_0t + \varphi) \tag{4.22}$$

where$|a_1|e^{j\varphi} = a_1$. In case$R_n = R_m = R$ and $C_k = C_l = C$ one has an RC oscillator with $\omega_0 = 1/RC$.

For a numerical application AD-IC based metamutator is selected and for obtaining a sinusoidal waveform with frequency of 16kHz, the values of capacitors and resistors were selected as $C_k = C_l$=10nf and $R_n = R_m$=1kΩ.

The output waveform resulting from the post layout simulation of the circuit in Figure 4.15 is given in Figure 4.16. As for AD-IC, TSMC, 0.25μm CMOS process parameters were used with transistor dimensions as shown in Table 3.6 and the

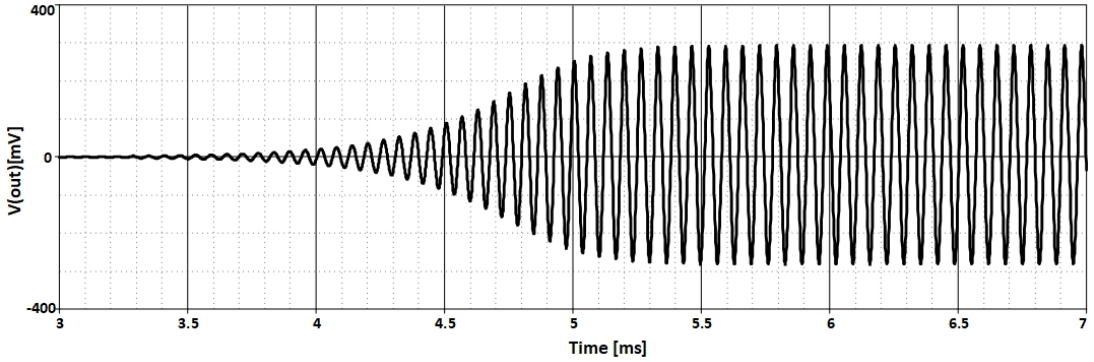


Figure 4.16: Simulation result of RC-oscillator

circuit in Figure 3.48. The supply voltages were chosen as ±1.25V and V_B as 0.8 V.

4.2 Realization of 2-Ports

In 2-port realizations, by properly terminating two of the metamutator ports the resulting circuit will behave as a desired 2-port from the remaining ports. First such 2-port realizations were introduced in [120]. In the sequel, new 2-port realizations will be given with a list, by no means complete, in Table 4.5.

4.2.1 Transconductance Amplifier

Another recent application of AD-IC based metamutator is its use in the design of Transconductance Amplifiers which relates the output port current to the input port voltage which was first given in [120] using Add-Subtract circuits. By connecting one resistor and one AC voltage source (V_s) to two of the ports and applying open circuit to the third port according to Table 4.5 the current in the fourth port will be equal to the V_s multiplied by the conductance in the other port.

Application	Realization	Port n	Port l	Port m	Port k
Transconductance Amplifier	#1	R_n	R_l	V_s	Open
	#2	R_n	R_l	Open	V_s
	#3	V_s	Open	R_m	R_k
	#4	Open	V_s	R_m	R_k
Transimpedance Amplifier	#1	I_s	R_l	R_m	Open
	#2	R_n	I_s	Open	R_k
	#3	R_n	Open	I_s	R_k
	#4	Open	R_l	R_m	I_s
Multifunctional Filter Voltage Mode	#1	R_3	$(C_1+ v_{S1}) \parallel (R_1+v_{S2})$	R_2+V_{s3}	C_2
	#2	C_2	R_2+V_{s3}	$(C_1+ v_{S1}) \parallel (R_1+v_{S2})$	R_3
	#3	$(C_1+ v_{S1}) \parallel (R_1+v_{S2})$	R_3	C_2	R_2+V_{s3}
	#4	R_2+V_{s3}	C_2	R_3	$(C_1+ v_{S1}) \parallel (R_1+v_{S2})$
Multifunctional Filter Current Mode	#1	R_3	$C_4 \parallel R_4 \parallel I_{in}$	R_1	C_2
	#2	C_2	R_1	$C_4 \parallel R_4 \parallel I_{in}$	R_3
	#3	$C_4 \parallel R_4 \parallel I_{in}$	R_3	C_2	R_1
	#4	R_1	C_2	R_3	$C_4 \parallel R_4 \parallel I_{in}$

TABLE 4.5: Different 2-port applications and realizations with metamutators

Applying realization #4 of Transconductance Amplifier in Table 4.5 to the metamutator with AD-IC, connecting V_s and R_m to ports l and m respectively, applying an open circuit to port n of the metamutator, the circuit in Figure 4.17 will

be obtained,

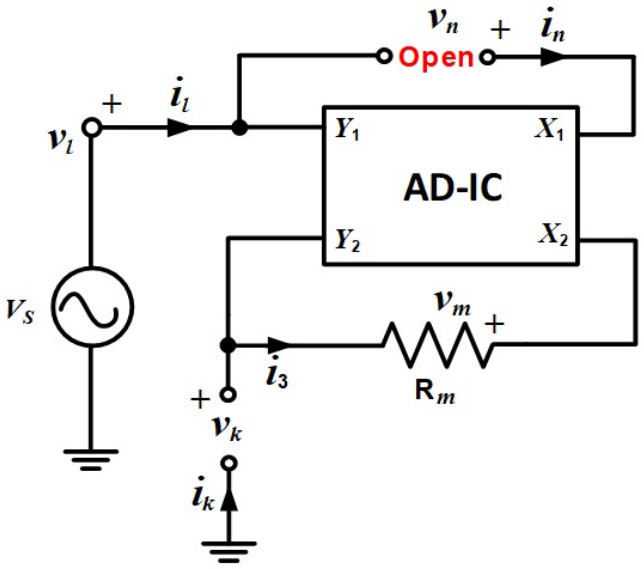


Figure 4.17: Transconductance amplifier realization #4

In this case according to (3.20), the current in port k will be equal to V_s multiplied by the conductance in port m as shown in:

$$i_k = -\frac{V_s}{R_m} \quad \Rightarrow \quad \mid A \mid = \mid \frac{i_k}{V_s} \mid = \frac{1}{R_m}(\mho) \tag{4.23}$$

Equality confirms the operation of the circuit in Figure 4.17 as a transconductance amplifier; the frequency domain I/O characteristics are given in Figure 4.18.

The metamutator was simulated using an AC voltage source with amplitude of 1V. As for AD-IC, TSMC, 0.25μm CMOS process parameters were used with transistor dimensions as shown in Table 3.6 and the circuit in Figure 3.48. The supply voltages were chosen as$\pm$1.25V and V_B as 0.8V. The values of R_k and R_m were selected as 10Ω and 10KΩ respectively. It can be observed that the circuit operates as transconductance amplifier for a wide range of frequency.

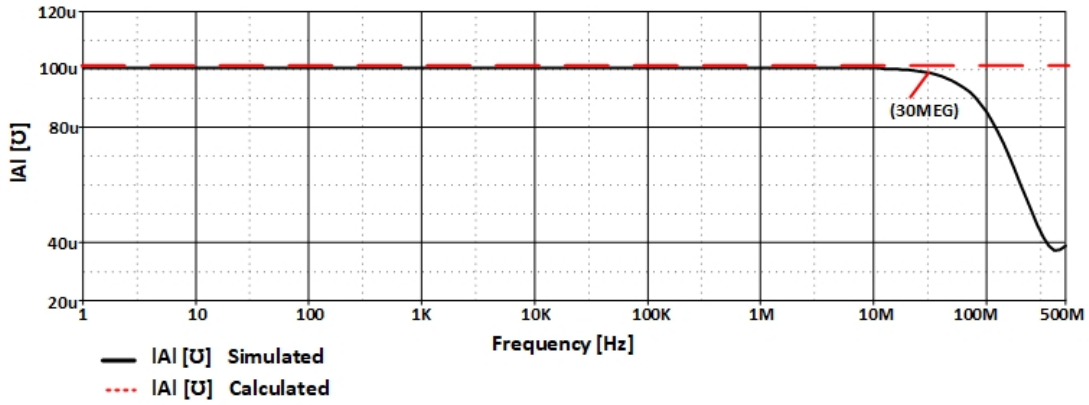


Figure 4.18: I/O characteristics vs. frequency of transconductance amplifier

4.2.2 Transimpedance Amplifier

Another recently proposed application of metamutators in [120] was the realization, using Add-Subtract circuits, of a Transimpedance Amplifier. Here the realization will be done using AD-IC based metamutator. By connecting one resistor and one AC current source (I_s) to two of the ports and applying open circuit to the third port according to Table 4.5 the voltage in the fourth port will be equal to I_s multiplied by the impedance in the other port.

Applying realization #2 of Transimpedance Amplifier in Table 4.5 to the metamutator with AD-IC, connecting I_s and R_n to ports l and n respectively then applying an open circuit to port m of the metamutator, the voltage in port k will be equal to I_s multiplied by the resistance in port n. The circuit of the resulting transimpedance amplifier is shown in Figure 4.19.

In this case, according to (3.20), the voltage at port k will be equal to I_s multiplied by the resistance in port n as shown with (4.24),

$$v_k = -R_n.I_s \quad \Rightarrow \quad \mid A \mid = \mid \frac{v_k}{I_s} \mid = \frac{1}{R_n}(\Omega) \tag{4.24}$$

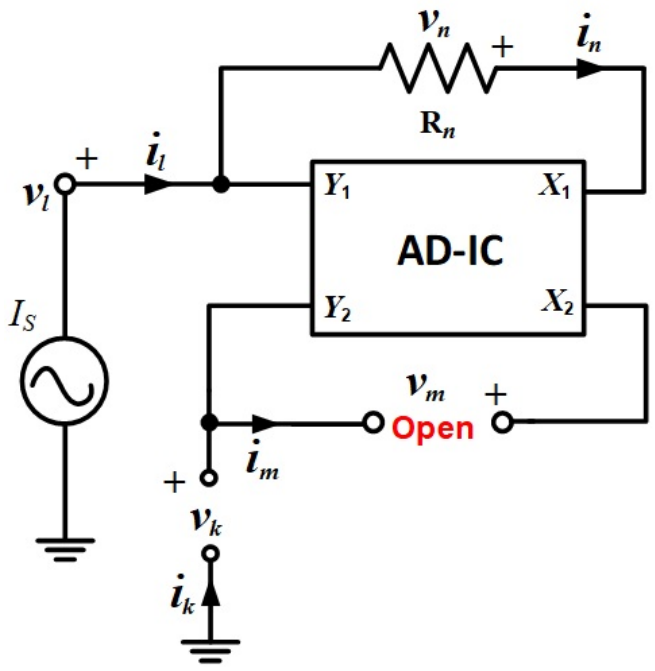


Figure 4.19: Circuit of transimpedance amplifier realization #2 of Transimpedance Amplifier

Equality (4.24) confirms the operation of the circuit in Figure 4.19 as transimpdance amplifier. Moreover, the frequency I/O characteristics are given in Figure 4.20.

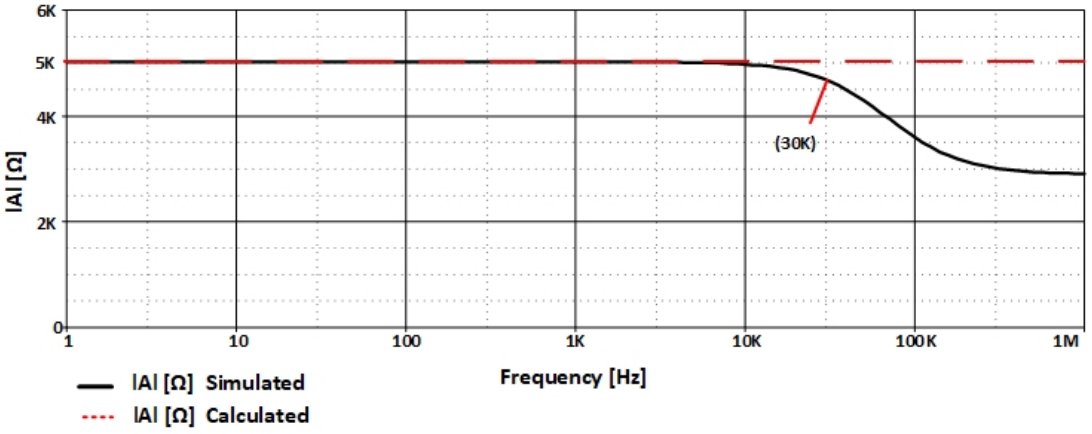


Figure 4.20: I/O characteristics vs frequency of transimpedance amplifier

The transimpedance amplifier of Figure 4.19 was simulated using an AC current source with amplitude of 100μA. As for AD-IC, TSMC, 0.25μm CMOS process

parameters were used with transistor dimensions as shown in Table 3.6 and the circuit in Figure 3.48. The supply voltages were chosen as ±1.25V and V_B as 0.8V. The values of R_n and R_k were selected as 5KΩ and 100MΩ respectively. It can be clearly observed that the circuit operates as a transimpedance amplifier in a wide frequency range.

4.2.3 Voltage Mode Multiple Input Single Output Universal Filter

Universal filters are popular as they can provide several filter functions with the same circuit and the literature on them is abundant; in [33-41] several multi input VM universal filters were introduced in contrast to [42-50] in which several multi output filters are being treated Different kinds of filters can be realized by proper selection of input voltage terminals in multi-input filters whereas different kinds of filters are realized by the selection of the output for multi-output filters. In this subsection VM-MISO filters will be treated.

However, these circuits suffer from one or more of the following problems:

i. In [36-37, 39-41] the necessity of passive component matching conditions,

ii. In [33-35, 38] lack of orthogonal controllability of the resonance angular frequency (ω_0) and quality factor (Q),

iii. In [37, 39-40] use of many passive components.

In this subsection a new application of metamutator as VM-MISO universal filters is being presented. Different realizations of this type of multifunctional filters using a metamutator were shown in Table 4.5. This new application will be illustrated by applying the realization in row #1 of multifunctional filter voltage mode in Table 4.5 to an AD-IC based metamutator.

The resulting block diagram of the universal filter obtained by applying realization in row #1 of multifunctional filter voltage mode in Table 4.5 is shown in Figure 4.21.

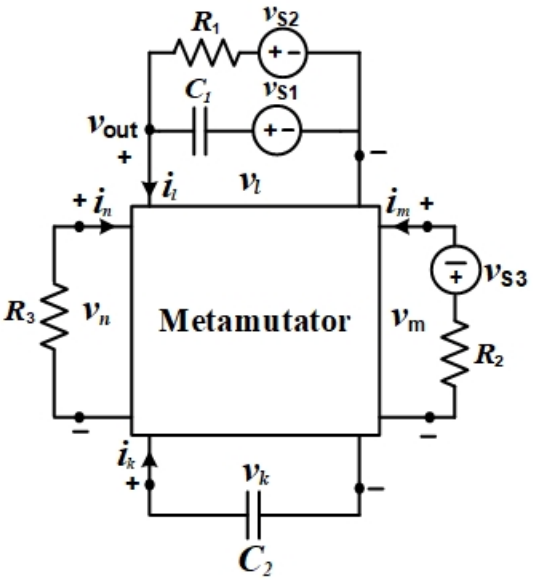


Figure 4.21: Universal filter structure

As the ports description matrices of all types of metamutators are the same, the proposed realizations of filters in Table 4.5 stand true for all of them. According to (1.9) the output voltage for VIM type metamutators, when all sources are present, is:

$$V_{out}(s) = \frac{s^2 C_1 C_2 R_1 R_2 R_3 V_{s1} + s C_2 R_2 R_3 V_{s2} + R_1 V_{s3}}{s^2 C_1 C_2 R_1 R_2 R_3 + s C_2 R_2 R_3 + R_1} \tag{4.25}$$

By connecting properly elements according to realization in row #1 of multi-functional filter voltage mode in Table 4.5 to AD-IC based metamutator the configuration will become as shown in Figure 4.22.

According to (1.9) and (3.20), $v_2 = v_3$ and assume that the output is $v_{out} = v_2 = v_3$ KCL at node A of the circuit in Figure 4.22 gives:

$$I_2 = sC_1(V_{s1} - V_{out}) + \frac{(v_{s2} - V_{out})}{R_1} \tag{4.26}$$

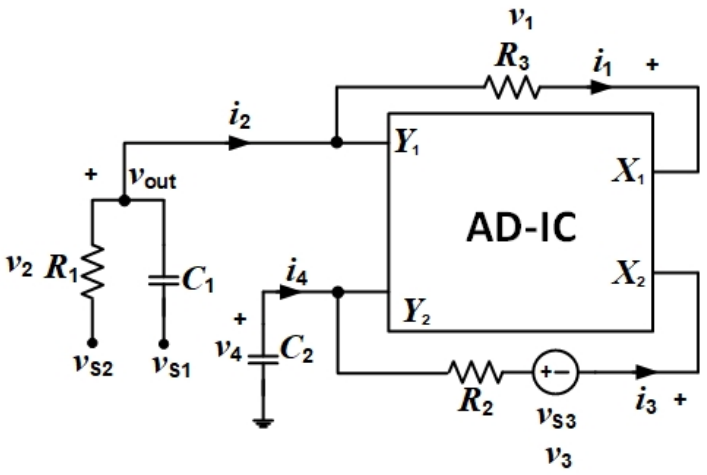


Figure 4.22: VIM based VM-MISO universal filter

Using $i_2 = i_1$ and $v_1 = -v_4$ from (3.20), $i_1 = -v_1/R_3 = v_4/R_3$ and $V_4 = (V_3 - V_{s3})/sR_2C_2$ in (4.26) gives:

$$V_3 - V_{s3} = s^2C_1C_2R_2R_3(V_{s1} - Vout) + \frac{sC_2R_2R_3}{R_1}(V_{s2} - V_{out}) \tag{4.27}$$

As $v_3 = V_{out}$, solving for V_{out} in terms of source voltages, the output voltage when all sources are present, is obtained as shown by (4.27) with the selection of various voltage sources resulting in different filter functions as illustrated by Table 4.6.

Selection	V_{s1}	V_{s2}	V_{s3}	**Filter Type**
#I	V_{in}	0	0	High-Pass
#II	0	0	V_{in}	Low-Pass
#III	0	V_{in}	0	Band-Pass
#IV	V_{in}	0	V_{in}	Band-Notch
#V	V_{in}	$-V_{in}$	V_{in}	All-Pass

TABLE 4.6: Different filter types depending on voltage source locations

All filter functions and their simulated characteristics will be displayed in Table 4.7 and Figure 4.23 respectively.

	Filter Function	Filter Type
1	$\frac{V_{out}}{V_{in}}(s) = \frac{s^2 C_1 C_2 R_3 R_2}{s^2 C_1 C_2 R_3 R_2 + s\frac{C_2 R_3 R_2}{R_1} + 1}$	High-Pass
2	$\frac{V_{out}}{V_{in}}(s) = \frac{1}{s^2 C_1 C_2 R_3 R_2 + s\frac{C_2 R_3 R_2}{R_1} + 1}$	Low-Pass
3	$\frac{V_{out}}{V_{in}}(s) = \frac{s\frac{C_2 R_3 R_2}{R_1}}{s^2 C_1 C_2 R_3 R_2 + s\frac{C_2 R_3 R_2}{R_1} + 1}$	Band-Pass
4	$\frac{V_{out}}{V_{in}}(s) = \frac{s^2 C_1 C_2 R_3 R_2 + 1}{s^2 C_1 C_2 R_3 R_2 + s\frac{C_2 R_3 R_2}{R_1} + 1}$	Notch
5	$\frac{V_{out}}{V_{in}}(s) = \frac{s^2 C_1 C_2 R_3 R_2 + s\frac{C_2 R_3 R_2}{R_1} + 1}{s^2 C_1 C_2 R_3 R_2 + s\frac{C_2 R_3 R_2}{R_1} + 1}$	All-Pass

TABLE 4.7: Transfer functions of different filters

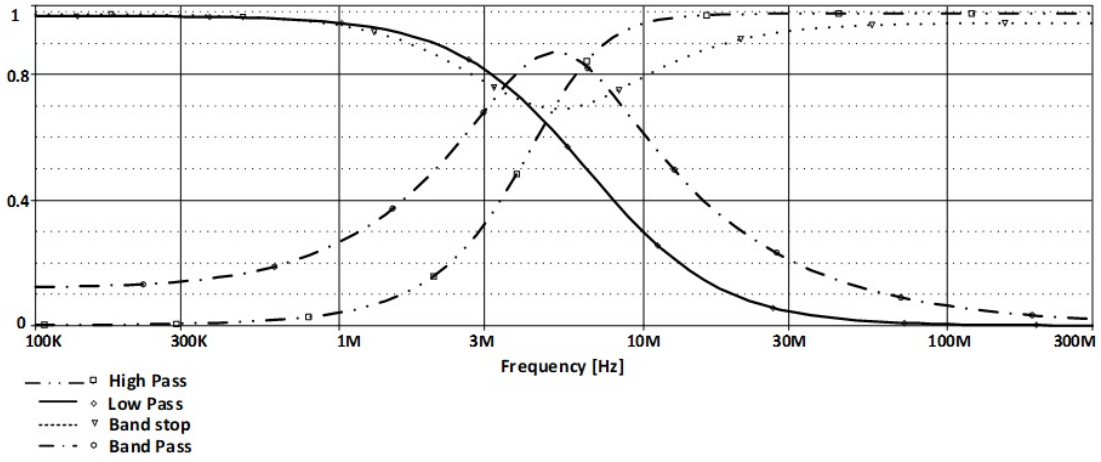


Figure 4.23: Simulation results of all filter types

The filter in Figure 4.22 was simulated by applying an AC voltage source with amplitude of 1 V to all inputs, one by one, following Table 4.5. For element values,$R_1 = R_2 = R_3$=1kΩ and $C_1 = C_2$= 25pF were taken. As for AD-IC,

TSMC, 0.25μm CMOS process parameters were used with transistor dimensions as shown in Table 3.6 and the circuit in Figure 3.48. The supply voltages were chosen as $\pm$1.25V and V_B as 0.8V.

There is no requirement for matching conditions in any of the filter realizations. The angular resonance frequency ω_0 and the quality factor Q of all filters are:

$$w_0 = \frac{1}{\sqrt{C_1 C_2 R_2 R_3}} \tag{4.28}$$

$$Q = R_1 \sqrt{\frac{C_1}{C_2 R_2 R_3}} \tag{4.29}$$

$$BW = \frac{w_0}{Q} = \frac{G_1}{C_1} \tag{4.30}$$

As shown by (4.28)-(4.30), the angular frequency can be controlled byR_2 and/or R_3 and the quality factor can be independently controlled by R_1. So the angular frequency and quality factor are orthogonally controllable. In this case, as $C_1 = C_2 = C$= 25Pf and $R_1 = R_2 = R_3 = R$= 1kΩ the angular frequency becomes $\omega_0 = 1/RC = 4.10^7(rad/s)$ and the quality factor is $Q = 1$.

Using expressions (4.28)-(4.30) sensitivities become,

$$S^{W_0}_{G_1,G_2} = -S^{W_0}_{C_1,C_2} = \frac{1}{2} \tag{4.31}$$

$$S^{Q}_{G_1} = -1, \quad S^{Q}_{G_2,G_3,C_1} = -S^{Q}_{C_2} = \frac{1}{2} \tag{4.32}$$

$$S^{BW}_{G_1} = -S^{BW}_{C_1} = 1 \tag{4.33}$$

The absolute values of calculated sensitivities are low and equal to unity only for bandwidth sensitivities.

4.2.4 Current Mode Single Input Multiple Output Universal Filter

CM filters have received significant attention due to their advantages such as higher frequency of operation, larger dynamic range, simpler circuitry and less power dissipation compared to their VM counterparts [42-47].

Universal filters are popular as they can provide several filter functions with the same circuit and the literature on them is abundant. To cite a few: in [47] a Single-Input Three-Output filter with four active devices (DOCCII) and five passive components, each DOCCII consisting of 20 MOS transistors, in [42] a Three-Input Single-Output filter with two active devices (CCCCTA) and two passive components, each CCCCTA consisting of 54 BJT transistors, in [43] a Three-Input Single-Output filter with two active devices (CFTA) and two passive components, each CFTA consisting of 25 MOS transistors, in [44] a Fully Differential Current Mode Universal Filter with seven active devices (CDCC) and two passive components, each CDCC consisting of 46 MOS transistors, in [45] a universal filter with single-input three-output only one active device FDCCII and four passive components, FDCCII consisting of 59 MOS transistors, in [46] a biquadratic filter with one active device (VDCC) and three grounded passive components, VDCC consisting of 22 MOS transistors, are given. All of these filters operate in Current Mode. Commercial monolithic IC universal filters such as LTC1562 [48], UAF42 [49] and MF10 [50] are also available.

In the sequel a new application of metamutator as CM-SIMO universal filter is being presented. Different realizations of this type of multifunctional filter have been shown in Table 4.8. This new application of CIM metamutator, will be investigated by applying the realization in row #4 of Table 4.8.

Realization	R_3	$C_4 \| \| R_4 \| \| I_i n$	C_2	R_1
#1	Port n	Port l	Port k	Port m
#2	Port k	Port m	Port n	Port l
#3	Port l	Port n	Port m	Port k
#4	Port m	Port k	Port l	Port n

TABLE 4.8: Multifunctional filter realizations

By applying realization #4 of Table 4.8 to AD-IC based metamutator, the circuit diagram of CM-SIMO universal filter will be obtained as shown in Figure 4.24.

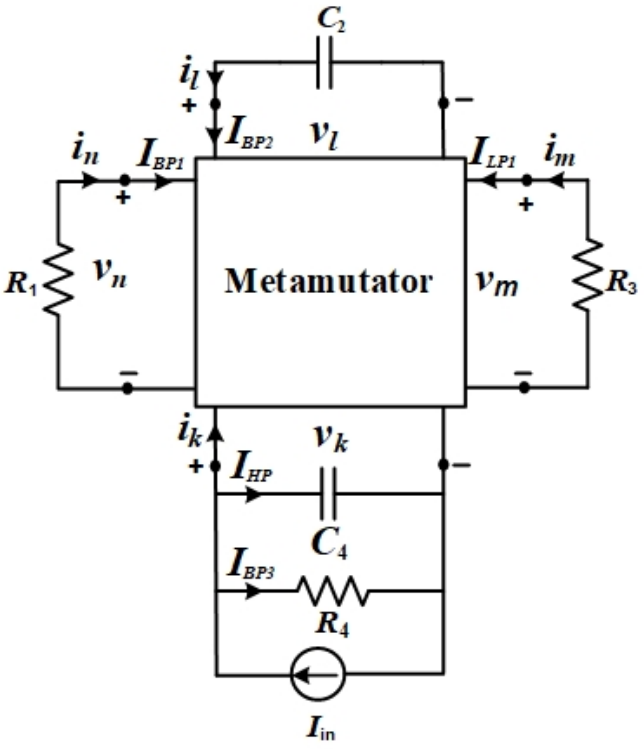


Figure 4.24: Circuit diagram of the CM-SIMO universal filter

For investigating the operation principle of CM-SIMO universal filter, the realization #4 is applied to the metamutator with AD-IC, as shown below,

Writing KVL, KCL and using element defining relations and solving for I_{BP1}, I_{BP2}, I_{BP3}, I_{LP1}, I_{LP2} and I_{HP} in terms of I_{in} results in filter functions as shown in Table 4.9.

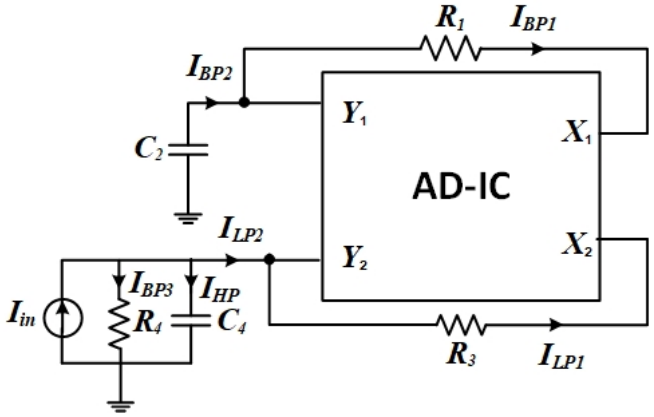


Figure 4.25: Current mode filter realization #4

Filter Type	Transfer Function
Band pass	$I_{AP}(s) = \frac{s^2 R_1 C_2 R_3 C_4 R_4 - s R_1 C_2 R_3 + R_4}{s^2 R_1 C_2 R_3 C_4 R_4 + s R_1 C_2 R_3 + R_4} I_{in}(s)$
Band pass	$I_{AP}(s) = \frac{s^2 R_1 C_2 R_3 C_4 R_4 - s R_1 C_2 R_3 + R_4}{s^2 R_1 C_2 R_3 C_4 R_4 + s R_1 C_2 R_3 + R_4} I_{in}(s)$
Low pass	$I_{AP}(s) = \frac{s^2 R_1 C_2 R_3 C_4 R_4 - s R_1 C_2 R_3 + R_4}{s^2 R_1 C_2 R_3 C_4 R_4 + s R_1 C_2 R_3 + R_4} I_{in}(s)$
High pass	$I_{AP}(s) = \frac{s^2 R_1 C_2 R_3 C_4 R_4 - s R_1 C_2 R_3 + R_4}{s^2 R_1 C_2 R_3 C_4 R_4 + s R_1 C_2 R_3 + R_4} I_{in}(s)$

TABLE 4.9: Transfer function of different filters

According to description matrix of metamutator as $i_1 = i_2$ and $i_3 = i_4$ so are $I_{BP1} = I_{BP2}$ and $I_{LP1} = I_{LP2}$. As seen from Table 4.9 the newly introduced current mode filter enables Low Pass, Band Pass and High Pass responses simultaneously. One can obtain the Band Stop filter by adding the I_{LP} and I_{HP} or an

All Pass filter by adding up the negative of I_{BP} to the sum of I_{LP} and I_{HP}. In these cases, the transfer functions become as given by (4.34) and (4.35) and the frequency behavior of all filters is shown in Figure 4.26.

$$I_{BS} = \frac{s^2 R_1 C_2 R_3 C_4 R_4 + R_4}{s^2 R_1 C_2 R_3 C_4 R_4 + s R_1 C_2 R_3 + R_4} I_{in} \tag{4.34}$$

$$I_{AP} = \frac{s^2 R_1 C_2 R_3 C_4 R_4 - s R_1 C_2 R_3 + R_4}{s^2 R_1 C_2 R_3 C_4 R_4 + s R_1 C_2 R_3 + R_4} I_{in} \tag{4.35}$$

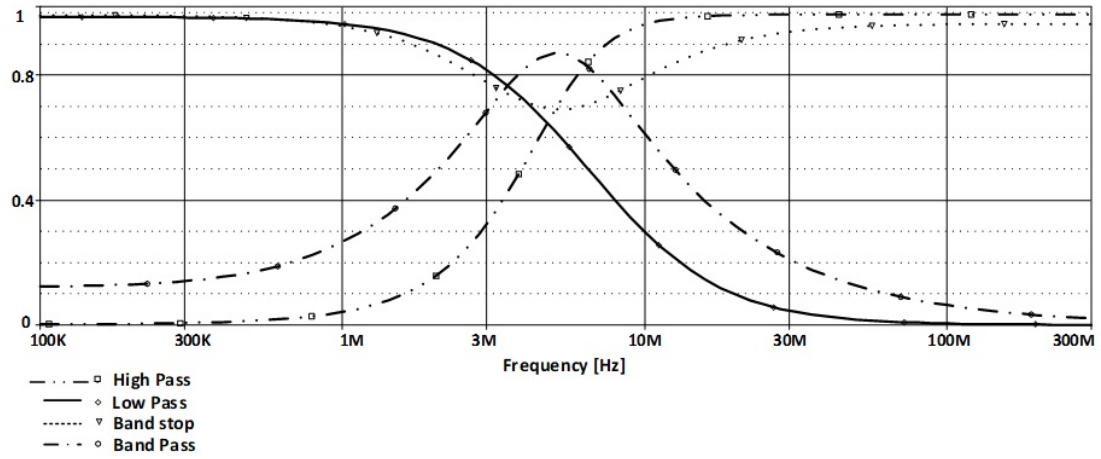


Figure 4.26: Simulation results of all type filters

The filter in Figure 4.25 was simulated by applying an AC current source with amplitude of 10mA to port 4 and selecting resistor and capacitor values as $R_1 = R_3 = R_4$=1kΩ and $C_2 = C_4$=10nF

following Table 4.8. As for AD-IC, TSMC, 0.25μm CMOS process parameters were used with transistor dimensions as shown in Table 3.6 and the circuit in Figure 3.48 The supply voltages were chosen as $\pm$1.25V and V_B as 0.8V.

The angular frequency ω_0 , quality factor Q and Bandwidth for all types of filters are obtained as:

$$w_0 = \frac{1}{\sqrt{R_1 C_2 R_3 C_4}} \tag{4.36}$$

$$Q = R_4\sqrt{\frac{C_4}{R_1 C_2 R_3}} \tag{4.37}$$

$$BW = \frac{w_0}{Q} = \frac{G_4}{C_4} \tag{4.38}$$

The quality factor (Q) and bandwidth are independent from angular frequency (ω_0) and can be independently adjusted by changing the value of passive component R_4.

In particular, choosing $C_2 = C_4 = C$ and $R_1 = R_3 = R_4 = R$ the angular frequency becomes $\omega_0 = 1/RC$ and the quality factor $Q = 1$. In this case all filters have non-inverting unity gain.

Using expressions (4.36)-(4.38) sensitivities become,

$$S^{W_0}_{G_1,G_3} = -S^{W_0}_{C_4,C_2} = \frac{1}{2} \tag{4.39}$$

$$S^{Q}_{G_4} = -1, \quad S^{Q}_{G_1,G_3,C_4} = -S^{Q}_{C_2} = \frac{1}{2} \tag{4.40}$$

$$S^{BW}_{G_4} = -S^{BW}_{C_4} = 1 \tag{4.41}$$

The sensitivities in (4.39)-(4.41) are all single parameter sensitivities e.g. $S^{(\omega_0)}_{(G_1,G_3)} = 1/2$ means that $S^{(\omega_0)}_{(G_1)} = S^{(\omega_0)}_{(G_3)} = 1/2$. The absolute values of calculated sensitivities are low and equal to unity only for bandwidth sensitivities.

Chapter 5

Two Operationally Nonlinear Applications of AD-IC

5.1 Analog Multiplier

Nonlinear building blocks like multipliers and dividers are widely used in several applications in analog signal processing. For example, applications such as mixers, modulators, adaptive filters. are composed of analog multipliers. In the literature different techniques have been applied for designing analog multipliers [51-59]. But, the growing interest in the design of fully integrated systems on chip encourages the inclusion of active blocks in their structures. Several analog multipliers using active building blocks are mentioned here.

In [51-52] second-generation Current Conveyors (CCIIs), in [53-54] Current Controlled Conveyors (CCCIIs), in [55] Dual-X Current Conveyors (DXCCIIs), in [56] current controlled current differencing buffered amplifiers (CCCDBAs), in [57-58] transconductors, in [59] Operational Transconductance Amplifiers (OTAs) are used for building analog multipliers.

However most of these analog multipliers suffer from one or more of the following disadvantages:

i. Excessive numbers of active devices [54], [59],

ii. Additional active or passive resistors [53],

iii. Complex internal circuitry of active device [54-56], [58],

iv. Appearance of the process parameters' dependent components at the output of the multiplier [55],

v. Excessive number of transistors [56-59].

Most of these realizations are not able to be fabricated as an integrated CMOS system on chip. For example, the circuits in [51-54], [56], [58-59] use bipolar or bipolar-JFET technology which involve more expensive processes. The complexity of the CMOS implementations given in [55] and [57] prevents the realization of the analog multipliers using commercially available CMOS circuits. Thus, it becomes a necessity to realize simple, compact fully CMOS multipliers.

In this section an AD-IC based voltage multiplier is offered. The operation principle of the newly proposed multiplier is based on squaring and subtracting the output voltages of AD-IC. The schematic block diagram of the proposed multiplier is shown with Figure 5.1.

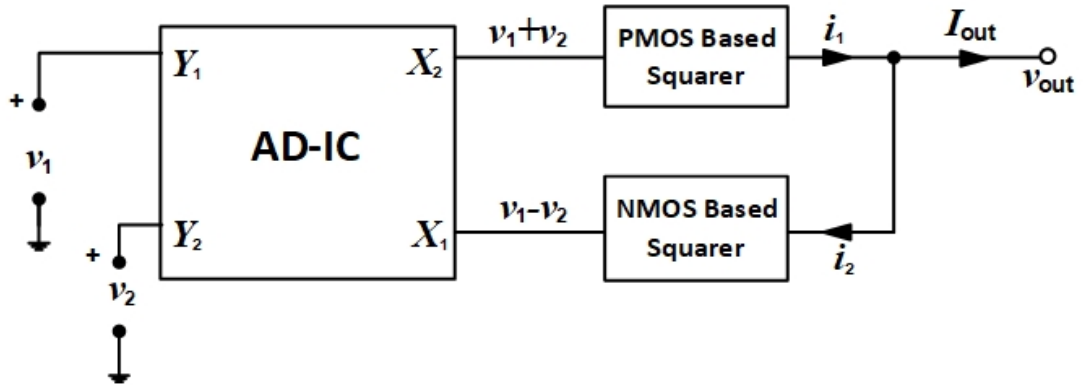


Figure 5.1: Block diagram of proposed multiplier

In the structure of proposed multiplier one AD-IC active element, a PMOS and an NMOS squarer circuits, consisting of two transistors each, are being used. According to (3.19),

$$\begin{cases} v_{x1} = v_{y1} - v_{y2} = v_1 - v_2 \\ v_{x2} = v_{y1} + v_{y2} = v_1 + v_2 \end{cases} \tag{5.1}$$

For NMOS and PMOS based squarer circuits the structures shown in Figure 5.2 (a) and (b) extracted from [60] are used. Transistor dimensions are given with Table 5.1.

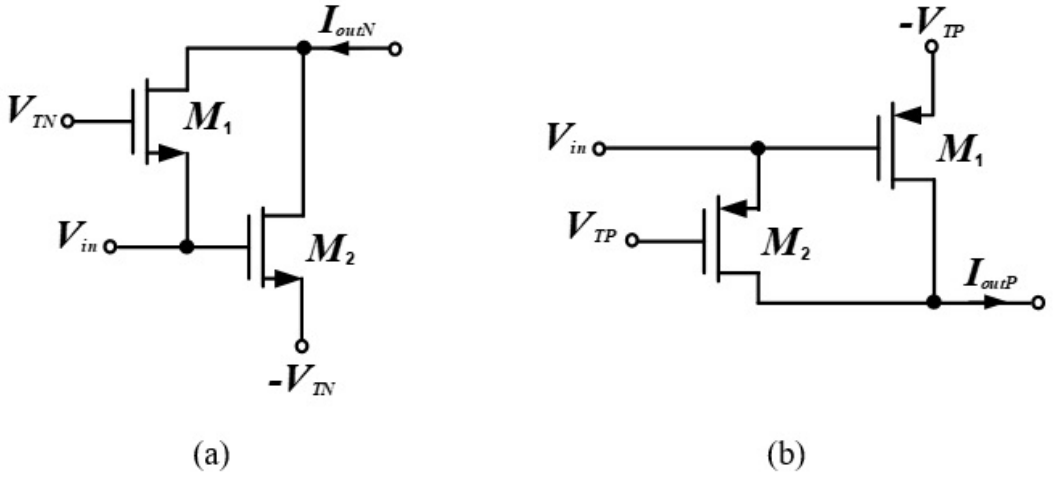


Figure 5.2: Voltage in/current out squarer circuits: (a) NMOS-based, (b) PMOS-based

NMOS Transistor	**W(μm)/L(μm)**
M_1, M_2	3.6/1.8
PMOS Transistor	**W(μm)/L(μm)**
M_1, M_2	3.6/1.8

TABLE 5.1: Transistor dimensions of the squarer circuits

When NMOS based squarer circuit is in positive cycle of v_{in}, M_1 is off and M_2 is in saturation region; when NMOS based squarer circuit is in negative cycle of v_{in}, M_2 is off and M_1 is in saturation region. Thus, the output current of the squarer for the whole cycle of input voltage is:

$$I_{outN} = \frac{1}{2} K_n {V_{in}}^2 \tag{5.2}$$

Here $K_{n1} = K_{n2} = K_n$ with $K_n = \mu_n C_{ox} \frac{W}{L}$ and W/L is the transistor aspect ratio, μ_n is electron mobility, and C_{ox} is the gate oxide capacitance per unit area and the threshold voltages V_{TN} of NMOS transistors are assumed to be equal.

When PMOS based squarer circuit is in positive cycle of v_{in}, M_2 is off and M_1 is in saturation region; when PMOS based squarer circuit is in negative cycle of v_{in}, M_1 is off and M_2 is in saturation region. Thus the output current of the squarer for the whole cycle of input voltage is:

$$I_{outP} = \frac{1}{2} K_p {V_{in}}^2 \tag{5.3}$$

Here $K_{p1} = K_{p2} = K_p$ with $K_p = \mu_p C_{ox} \frac{W}{L}$ and W/L is the transistor aspect ratio, μ_p is electron mobility, and C_{ox} is the gate oxide capacitance per unit area and the threshold voltages V_{TP} of PMOS transistors are assumed to be equal. So the currents i_1, i_2 and I_{out} in Figure 5.1 can be calculated as,

$$\begin{cases} I_{outN} = i_2 = \frac{K_n}{2}(v_1 - v_2)^2 \\ I_{outP} = i_1 = \frac{K_p}{2}(v_1 + v_2)^2 \end{cases} \tag{5.4}$$

$$I_{out} = i_1 - i_2 = [\frac{K_p}{2}(v_1 + v_2)^2 - \frac{K_n}{2}(v_1 - v_2)^2] \tag{5.5}$$

By selecting, $K_p = K_n = K$, the output current I_{out} can be expressed as,

$$I_{out} = 2K v_1 v_2 \tag{5.6}$$

By terminating the output of the multiplier with a resistor R_L, when a voltage mode operation is desired, the output voltage can be expressed as:

$$v_{out} = K_M v_1 v_2 \tag{5.7}$$

where $2R_LK = K_M$. As it can be seen from (5.6) and (5.7) the proposed multiplier can operate in both transconductance- and in voltage-mode.

The most significant application of multipliers being to operate as modulator, in the remainder of this section, AD-IC based multiplier circuit's Amplitude Modulation (AM) capability will be illustrated.

By applying two sinusoidal voltage sources with different frequencies, one as message signal and the other one as carrier signal, to the inputs of multiplier circuit, it will operate as a modulator. The simulation results are shown in Figure 5.3.

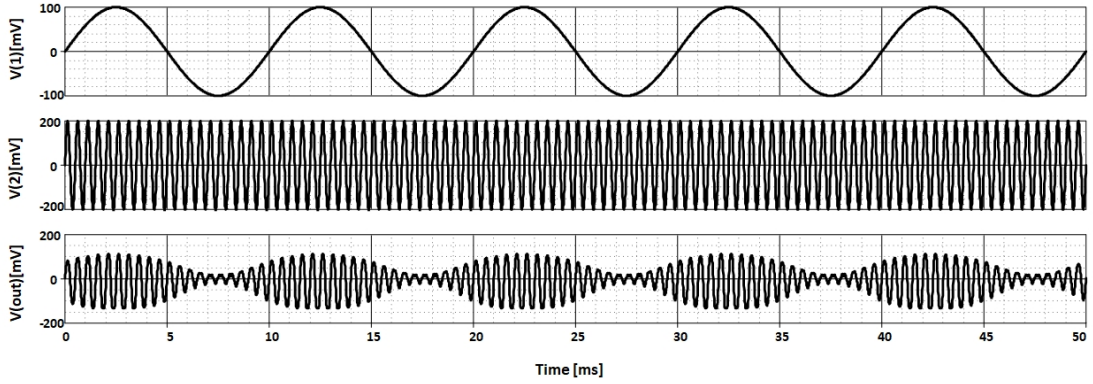


Figure 5.3: Simulation result of multiplier as modulator

The modulator circuit is simulated by applying two sinusoidal voltage sources, one as message signal with amplitude of 100mV and frequency of 100Hz and the other one as carrier signal with amplitude of 200mV and frequency of 2000Hz. As for PMOS and NMOS squarer circuits transistors with process parameters TSMC, 0.18μm CMOS were used with dimensions as shown in Table 5.1 and the circuit structures proposed in Figure 5.2; supply voltages were chosen as $\pm$0.4V. For AD-IC, TSMC, 0.25μm CMOS process parameters were used with transistor dimensions as shown in Table 3.6 and the circuit in Figure 3.48, the supply voltages were chosen as $\pm$1.25V and V_B as 0.8V. v_{out} in Figure 5.3 confirms the operation of the AD-IC based multiplier as modulator.

5.2 Full-Wave Rectifier

Precision rectifiers are widely used in many fields such as analog signal processing, control engineering, communications and also in measurement applications and instrumentation such as AC voltmeters and ammeters, averaging circuits, signal-polarity detectors, peak-value detector rectifications [61-62].

In general rectifier circuits, consisting of diodes and several passive components exist in the literature but because of the threshold voltage limitations of diodes, which are about 0.3V and 0.7V for germanium and silicon diodes respectively, the usage of these types of rectifiers for high-precision and low-voltage applications are not suitable. Consequently, for high-precision rectification and/or achieving wider frequency response ranges, active elements have been used. Many different topologies of rectifiers, with one or more active IC devices in their structures, have been introduced in [63-81]. However, these circuits suffer from one or more of the following disadvantages:

i. quite a large number of transistors,

ii. high area occupancy,

iii. high power consumption [69-78],

iv. and necessity of satisfying different element matching conditions [63-69].

By connecting terminal y_1 of AD-IC to ground, applying a voltage source as input to terminal y_2 and connecting diodes D_1 and D_2 to terminals x_1 and x_2 respectively the structure of the proposed voltage mode full-wave rectifier will become as shown in Figure 5.4. The most important feature of the proposed circuit is its simple structure containing only twelve NMOS transistors and two diodes.

To see that the configuration in Figure 5.4 operates indeed as a full wave rectifier consider the following:

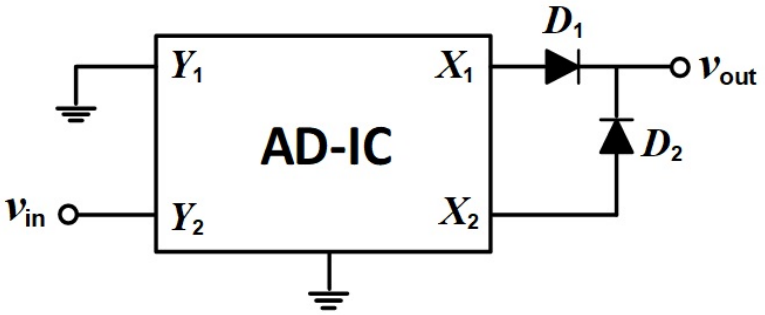


Figure 5.4: Block diagram of AD-IC

- As one can observe the terminal y_1 is grounded hence $v_{y1} = 0$ and in this case, v_{x1} which is equal to $v_{y1} - v_{y2}$ will be equal to $-v_{in}$.
- on the other hand v_{x2} which is equal to $v_{y1} + v_{y2}$ will be equal to v_{in}.

When the input of the proposed full-wave rectifier has positive values, denoted by $v_{in}(t)_+$, the voltage at terminal x_1 is equal to $-v_{in}$ and the voltage at terminal x_2 is equal to v_{in}, so D_1 is off and D_2 is on yielding:

$$v_{out}(t) = v_{in}(t)_+ \tag{5.8}$$

When the input of the proposed full-wave rectifier has negative values, denoted by $v_{in}(t)_-$, the voltage at terminal x_1 is equal to v_{in} and the voltage at terminal x_2 is equal to $-v_{in}$, so D_1 is on and D_2 is off giving:

$$v_{out}(t) = -v_{in}(t)_- \tag{5.9}$$

The input voltage of the proposed full-wave rectifier can be expressed as,

$$v_{in}(t) = v_{in}(t)_+ + v_{in}(t)_- \tag{5.10}$$

From (5.8), (5.9) and (5.10) it can be concluded that the output voltage of proposed full-wave rectifier can be given as,

$$v_{out}(t) =\mid v_{in}(t) \mid \tag{5.11}$$

which proves that the circuit proposed in Figure 5.4 operates as a full-wave rectifier. The proposed AD-IC based rectifier circuit has the following advantages:

i. Voltage-mode operation,

ii. Low-output, high-input impedances which make it suitable for IC fabrication without the need of any additional buffer circuits,

iii. Fewer CMOS transistors with respect to rectifiers in [64-78],

iv. No resistors are used hence there is no need of resistive matching conditions.

By applying a sinusoidal voltage source with amplitude of 100 mV and frequency of 1kHz to the input of the circuit in Figure 5.4, the time domain waveforms of v_{in} and v_{out} and, the DC transfer characteristic of the full-wave rectifier are shown in Figure 5.5 and Figure 5.6 respectively. For diodes D_1 and D_2 the 1N4148 model is used. The supply voltages are chosen as $\pm$1.25V and V_B as 0.8V.

From both, Figure 5.5 and Figure 5.6 it can be seen that the output waveform and the DC characteristic of the proposed rectifier are in very good agreement with the expected behavior.

Another set of parameters to evaluate the behavior of the proposed full-wave rectifier and enable its comparison with other full-wave rectifier circuits are the DC value transfer (P_{DC}) and RMS error (P_{RMS}). These values are defined with (5.12) and (5.13) respectively where $v_{oa}(t)$ and $v_{oi}(t)$ represent the actual and ideal output signals of rectifier and T is the period of the rectified signal. (5.12)

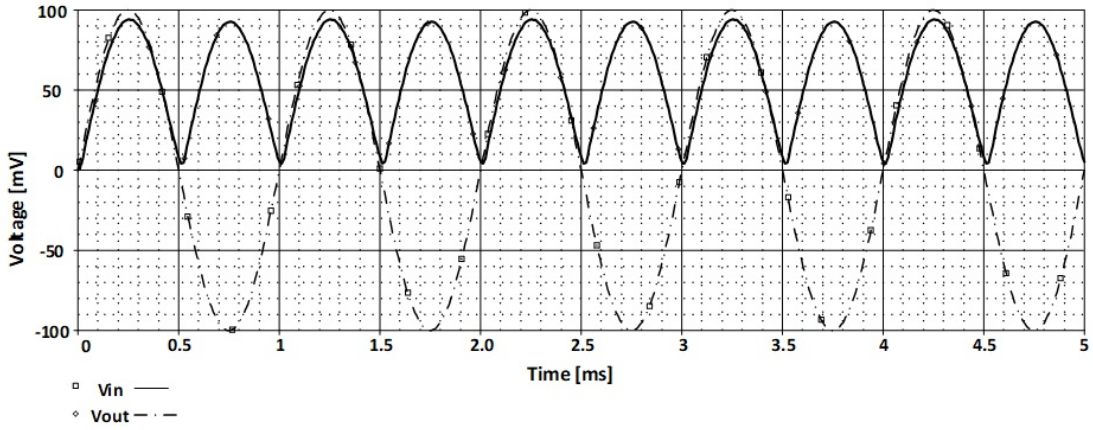


Figure 5.5: Time-domain input and output waveforms of the rectifier with AD-IC

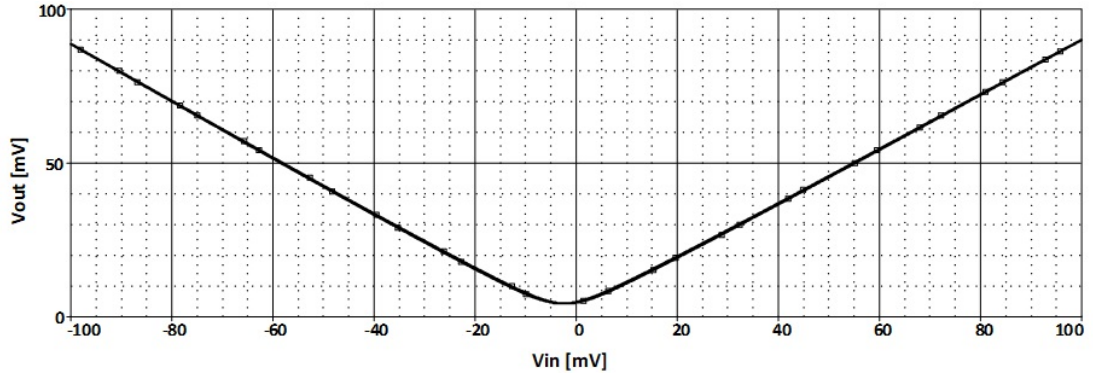


Figure 5.6: DC characteristics of the non-inverting full-wave rectifier circuit

and (5.13) imply that the ideal values for P_{DC} and P_{RMS} are unity and zero respectively.

$$P_{DC} = \frac{\int_T v_{oa} t dt}{\int_T v_{oi} t dt} \tag{5.12}$$

$$P_{RMS} = \sqrt{\frac{\int_T [v_{oa}(t) - v_{oi}(t)]^2 dt}{\int_T v_{oi}^2(t) dt}} \tag{5.13}$$

The characteristics in Figure 5.7 clearly show that as the input frequency increases, the value of P_{DC} decreases and that of P_{RMS} increases due to the non-ideal effects present in the rectifier. In order to show how well the newly proposed

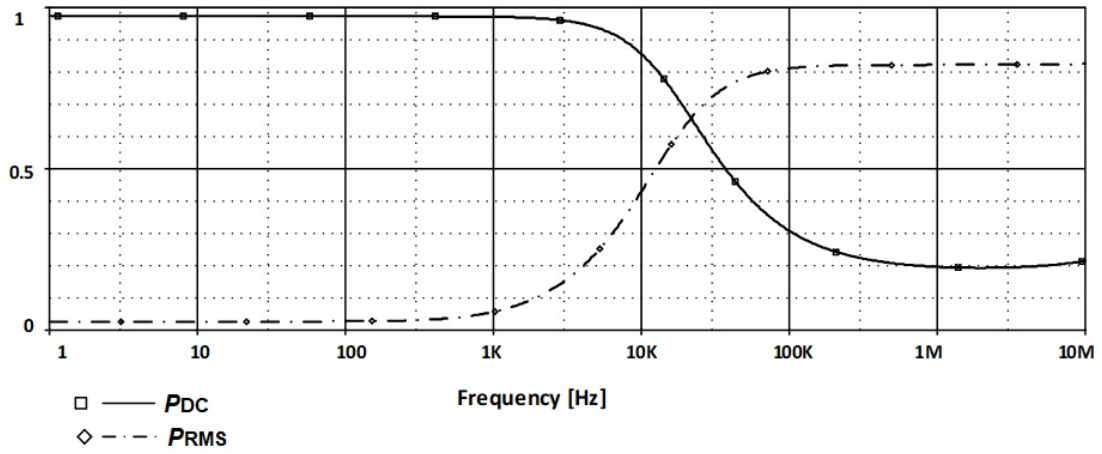


Figure 5.7: P_{DC},$P_{(RMS)}$ characteristics of the rectifier in 100mV input amplitude

rectifier circuit with AD-IC behaves, a comparison with previously published rectifiers has been presented in Table 5.2.

paper	#of ICs	#of Transistors	#of Resistors	High In / Low Out Impedance	Res. Match Required
[64]	2 OTA	>> 12	7	NO/YES	YES
[66]	2 CCII	>> 12	2	YES/NO	YES
[68]	1 CCII-	15	2	NO/NO	YES
[69]	1CCII,1 DXCCII	29	2	YES/NO	YES
[70]	2 CCII	36	2	YES/NO	YES
[71]	1 DO-OTA	24	1	YES/NO	NO
[72]	1 CCII,1 OpAmp	41	3	YES/YES	YES
[73]	2 CCII	80	3	YES/NO	YES
[74]	2 CCII	36	2	YES/YES	YES
[75]	2 CCII	42	2	YES/NO	NO
[76]	2 CCII,1 Buffer	26	4	YES/NO	YES
[77]	2 DVCC	24	26	YES/YES	YES
[78]	4 CCCII	60	5	YES/NO	YES
[79]	2CFOA, 3/2NMOS	39/38	0/1	YES/YES	YES
Here	1AD-IC	12	2	YES/YES	NO

TABLE 5.2: Comparison of the proposed rectifier with others

Chapter 6

Conclusion

A brief introduction to basic circuit elements together with a new class of memory elements namely, memstors were presented in the first chapter. Also, the necessity of using mutators together with previously developed mutator circuits in literature was considered. A brief overview of 4-port metamutators according to their port description matrices, their classification into two categories: Voltage Inverting Metamutator (VIM) and Current Inverting Metamutator (CIM) were presented.

The necessity of using mutators and the basic definition of 2-port mutators with their port relation matrices and different kind of mutators for mutating nonlinear circuit elements to memristors or converting memristors to other non-volatile circuit elements like meminductor and memcapacitor, also some of the previously developed classical mutator circuits well-known in the literature, were presented in the second chapter.

Many incognito mutator-like 4-ports hidden in the simulations/emulations of devices in the literature have been uncovered and named metamutator in the third chapter. In addition to introducing some of these incognito metamutator realizations, newly designed metamutator circuits with one or two active devices, with their ports relation matrices and their different realization tables were presented. Also a novel realization of a metamutator with single active device, Additive and Differential IC (AD-IC) was proposed and implemented with twelve transistors only; a minimal number among all realizations.

In the fourth chapter, different applications of metamutators developed during the research period of this thesis were presented. As the port description matrix of all introduced metamutators in Chapter 3 are the same, these applications stand true for all of metamutator realizations. Depending on how some of the ports are terminated, many metamutator applications, which can be classified into two groups, is attained:

I. 1-port circuits realized with metamutators,

II. 2-port circuits realized with metamutators.

It has been shown in this chapter that in 1-port realizations, by properly terminating three ports of the metamutator the resulting circuit behaves like a mutator, floating and/or grounded impedance scalor, oscillator. In addition, fourth chapter also contains new 2-port realizations: transconductance/transimpedance-amplifiers, voltage mode multiple input single output universal filters and current mode single input multiple output universal filters. Also, a list of all of these applications were demonstrated with Table 1.3 and Table 4.5. The advantages of the introduced circuits were demonstrated and these applications were verified in detail with PSPICE simulations using transistor parameters obtained from layout level descriptions of metamutators. Comparisons between simulation and theoretical results were also presented.

In the fifth chapter, two new applications: a voltage multiplier with single AD-IC and two squarer circuits consisting of two transistors each, and a full-wave rectifier again with only an AD-IC and two diodes in its configuration were presented. Both of the circuits were simulated with parameters extracted from the layout and have shown very good conformity with ideal voltage multiplier and full-wave rectifier behaviors. Also detailed comparison tables of the proposed analog multiplier and full-wave rectifier with others existing in the literature, were included in this chapter.

Future work will concentrate on the comparison of VIM versus CIM, novel types of metamutators, their different realizations, tuning with external elements to improve the behavior of these circuits and further applications. Comparing the effects of using different kind of metamutators in the design of filters realized here will deserve special consideration.

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