# Micromachined capacitive transducer arrays for intravascular ultrasound

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#### ABSTRACT

Intravascular ultrasound (IVUS) imaging has become an essential imaging modality for the effective diagnosis and treatment of cardiovascular diseases during the past decade enabled by innovative applications of piezoelectric transducer technology. The limitations in the manufacture and performance of the same piezoelectric transducers have also impeded the improvement of IVUS for emerging clinically important applications such as forward viewing arrays for guiding interventions and high resolution imaging of arterial structure such as vulnerable plaque and fibrous cap, and also implementation of techniques such as harmonic imaging of the tissue and of the contrast agents. Capacitive micromachined ultrasonic transducer (CMUT) technology shows great potential for transforming IVUS not only to satisfy these clinical needs but also to open up possibilities for low-cost imaging devices integrated to therapeutic tools. We have developed manufacturing processes with a maximum process temperature of 250°C to build CMUTs on the same silicon chip with integrated electronics. Using these processes we fabricated CMUT arrays suitable for forward viewing IVUS in the 10-20MHz range. We characterized these array elements in terms of pulse-echo response, radiation pattern measurements and demonstrated its volumetric imaging capabilities on various imaging targets.

Keywords: Micromachined ultrasonic transducers, intravascular ultrasound imaging

# 1. INTRODUCTION

Although the value of angiography remains unquestioned, radiographic imaging depicts a two-dimensional silhouette of the arterial lumen and has many limitations. While several competitive technologies such as optical coherence tomography and magnetic resonance imaging are under development, currently intravascular ultrasound (IVUS) represents the gold standard in the assessment of the extent of coronary artery disease, the leading cause of death in the U.S.<sup>1</sup> IVUS provides the unique possibility to image the arterial vessel wall *in vivo*, allowing one to study the coronary morphology during life and over time. IVUS can be used to assess the compensatory enlargement of coronary arteries in response to atherosclerotic plaque accumulation<sup>2</sup>. Repeated IVUS investigations allow tracking the natural course of atherosclerotic lesions and effects of therapeutic measures such as lipid-lowering therapy<sup>3</sup>. IVUS also plays an important role in the mechanistic assessment of treatments such as balloon angioplasty, stent implantation, and more recently drug eluting stents<sup>4-6</sup>. Clinically driven emerging techniques, such as volumetric imaging, de-correlation based flow measurements<sup>7</sup>, ultrasonic elastography<sup>8,9</sup>, and characterization and identification of vulnerable plaque<sup>10,11</sup> indicate that the role of IVUS in the diagnosis and treatment of coronary artery disease will continue to grow in the near future. These new techniques require IVUS systems to generate images with higher resolution, higher frame rates and also to have sensitivity over a broad frequency range to allow harmonic imaging.<sup>12</sup>

Piezoelectric transducer technology, which forms the basis of current IVUS systems, has severe limitations. Although significant resources has been used for the development of piezoelectric materials over the last 30 years, the IVUS

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systems based on single piezoelectric transducers and rotating reflectors such as shown in Fig. 1-A have 20-50% fractional bandwidth around 40MHz<sup>13-</sup> <sup>15</sup>. Manufacturing difficulties force synthetic phased array IVUS catheters to operate only at 20MHz with 20-30% fractional bandwidth<sup>16,17</sup> (Figure 1-B). The axial resolution of these systems is 100-120 µm, clearly not adequate for the assessment of the cap thickness of rupture-prone plaque. A critical value of at least 65µm in thickness to withstand circumferential stresses has been reported<sup>18</sup>.

Piezoelectric transducers also limit the geometry of IVUS arrays that can be



Figure 1. A) Schematic diagram of the current side-looking IVUS with single piezoelectric transducer with rotating mirror or transducer. (B) Schematic of the 64-element solid state array with wire bonded integrated electronics. The transducer array is driven by 4 silicon chips each controlling 16 channels for transmit and receive operations. Adopted from reference 15.

realized. For example, despite serious efforts, it has not been feasible to reliably fabricate ring annular piezoelectric transducer arrays for forward looking IVUS<sup>19</sup>. Even 1-D piezoelectric arrays for small animal imaging, which have more relaxed geometrical constraints, have proven difficult to build<sup>20</sup>. In addition to fabrication problems which increases catheter cost, piezoelectric transducers cannot be directly integrated with silicon integrated circuits (IC) to realize IVUS arrays with smaller dimensions. For example, both the length and the diameter of the IVUS probe can be reduced significantly in the solid state arrays such as shown in Fig. 1-B, if the transducer array can be directly built on the CMOS electronics chips. This would fulfill the clinical need for smaller IVUS probes interrogating not only large arteries but smaller branches, as well as probes with better crossing characteristics in order to navigate through side-branches with sharp take-off or sharply curved arteries. Furthermore, this approach would yield simpler, low cost IVUS probes which could potentially allow IVUS imaging during balloon angioplasty or stent delivery operations.

In this paper, we first give a background on CMUTs and discuss various approaches for device fabrication and electronics integration. We then describe the low temperature fabrication process that we have developed for post-CMOS fabrication of CMUTs. We present results of transducer characterization efforts and initial imaging results obtained from ring-annular forward looking IVUS arrays operating around 15MHz.

# 2. CAPACITIVE MICROMACHINED ULTRASONIC TRANSDUCERS

Micromachined transducers based on a different principle have the potential to enable both low-cost, low-profile, and advanced IVUS probes. CMUTs, which have been developed during the past decade, provide improved performance over piezoelectric transducers especially for imaging arrays with small dimensions<sup>21,22</sup>. The basic CMUT structure consists of a dielectric membrane with a metal layer (buried or on the surface of the membrane) suspended above a highly doped silicon substrate, or an electrode as shown schematically in Fig. 2-A. When a voltage is applied between the membrane and the silicon substrate, electrostatic forces attract the membrane towards the substrate and the stress within the membrane resists the attraction. If the membrane is driven by an alternating voltage, ultrasound is generated in the medium in contact with the membrane. Since the electrostatic force is always attractive, a DC bias voltage is applied to the capacitor to have a linear operation<sup>23</sup>. Microfabrication techniques based on semiconductor microelectronics manufacturing processes enable control of dimensions of CMUTs with very high precision. Therefore, fabrication of 1-D and 2-D CMUT imaging arrays of different size and shape involves just several standard photolithographic steps connecting the cells in a particular pattern. Figure 2-B shows a test structure with 4 elements of a ring-annular forward-looking CMUT-based 15MHz IVUS array <sup>24</sup>. Note that the membrane width is around 40µm and the optimized buried top electrodes cover ~75% of the membrane, which are connected by 3µm wide traces. The

thickness of the silicon nitride membrane is between 0.5-  $1\mu m$  and the vacuum sealed cavity gap thickness is in the range of 50-100nm<sup>25</sup>.

CMUTs have inherent advantages especially for ultrasonic imaging arrays. While piezoelectric transducers are resonant devices requiring matching layers to efficiently couple to fluids and backing materials for broadband operation<sup>26</sup>, the CMUT is inherently a *non-resonant, broadband device* which can provide higher depth resolution in ultrasound images. In addition, microfabrication techniques enable one to tailor the response of the CMUT through parameters such as the DC bias, gap thickness, size and location of the electrode(s), membrane thickness and mass distribution. As discussed below, we have developed systematic methods to exploit these unique fabrication capabilities to enhance CMUT performance for particular IVUS applications. In contrast, the design of a piezoelectric transducer is strictly limited by the operating frequency and intrinsic material constants.

Perhaps the most important advantage of CMUT technology for IVUS is its potential for electronics integration. Electronics integration helps both in miniaturization of IVUS arrays and also minimizes the effect of parasitic capacitance which is detrimental to the operation of IVUS with small arrays elements such as the  $40\mu m \times 120\mu m$  elements shown in Fig. 2-B.

There are several approaches to CMUT-electronics integration depending on the CMUT fabrication process. When a high temperature process such as Low Pressure Chemical Vapor Deposition (LPCVD) step is used to deposit the silicon nitride dielectric layer at 800°C or higher, CMOS electronics cannot be integrated to the CMUT array on the same silicon chip<sup>27</sup>. Alternatively, the CMUT membranes can be formed from single crystal silicon using wafer bonding<sup>28</sup> at 1100°C. These processes require a hybrid integration approach where a through-wafervia is also fabricated on the CMUT wafer to connect each CMUT array element on the top side of a silicon wafer to a bond pad at the bottom of the wafer. The electrical connectivity is provided by a doped polysilicon layer deposited by a high temperature (> 700°C) LPCVD step<sup>29,30</sup>. The CMUT wafer is then be



Figure 2. A) Schematic of a single cell of a CMUT. B) A typical cMUT on silicon with vacuum sealed cavities. This test structure consists of 4 ring-annular array elements

flip-chip bonded to another silicon wafer containing the IC electronics<sup>31</sup>. The main disadvantages of this approach are the complex through wafer via process and bonding process, the voltage restrictions due to p-n junction operation and the need for at least two wafers, which may not be acceptable in terms of cost and size in case of IVUS catheters.

An alternative approach for IVUS arrays is monolithic integration of CMUTs with CMOS electronics. In this case the CMUTs are formed on the same silicon substrate with the CMOS electronics either simultaneously or after CMOS electronics is developed (Post-CMOS processing). When the CMUTs are fabricated along with electronics, the CMUT membranes occupy a large surface area requiring large die sizes<sup>32</sup>. This is not cost-effective, and has severe drawbacks for densely populated 2-D arrays and IVUS applications.

Our approach to CMUT-IC integration is to use "Post-CMOS processing". Post-CMOS processed, single chip micromachined gas and chemical sensors, very dense 2-D micromirror arrays have already been demonstrated<sup>33,34</sup>. The

key is to this approach is the use of low-temperature processes (maximum temperature below 400°C) to build the CMUT on top of the existing CMOS circuitry, so that the performance of the electronics is not compromised. A possible Post-CMOS processed CMUT cross section is shown in Fig. 3, where a silicon dioxide layer is deposited over the CMOS circuitry for electrical isolation and it is planarized using chemical mechanical polishing (CMP). This technique is already used to manufacture digital mirror displays by Texas Instruments, which is one of the most successful MEMS products<sup>34</sup>. In the case of CMUT arrays, the devices are fabricated on the flat silicon dioxide surface using low temperature plasma enhanced chemical vapor deposition (PECVD) and metal deposition techniques. As will be described below, we have



Figure 3. Schematic cross-section of a CMUT fabricated on CMOS electronics using Post-CMOS processing.

recently developed a process where high performance CMUTs for IVUS are fabricated using a maximum process temperature of 250°C<sup>25</sup>. More recently, Sensant Corporation has succeeded in building 1-D CMUT arrays at 3.5MHz over a commercial CMOS circuit containing high voltage IC <sup>35</sup>. This is a significant milestone proving the feasibility of all-silicon single chip CMUT arrays for ultrasound imaging.

Note that one can easily extend this fabrication scheme to build CMUT IVUS arrays directly on the silicon chip carrying the IVUS electronics such as shown in Fig. 1 B. Each of these ICs control 16 channels of the 64-element synthetic phased array IVUS, and it has been key to the success of this probe<sup>36</sup>. Since microelectronics has developed significantly after the introduction of that particular CMOS chip in 1994, we can expect to increase the frequency range or enhance the functionality of these CMUT-CMOS integrated IVUS probes. Also, the economics of this approach is clear: Over 5000 IVUS array chips can be obtained from one 15cm diameter silicon wafer with high yield, resulting in a cost of around \$1 per chip.

#### 3. LOW TEMPERATURE CMUT PROCESSING

A critical capability required for CMUT-based IVUS arrays monolithically integrated with electronics is the low temperature fabrication of CMUTs with desired characteristics. We have fabricated CMUTs operating in the 5MHz to 40MHz range with maximum process temperature of 250°C <sup>25,37</sup>. Each step of this CMOS compatible process is well





characterized and shown to produce CMUTs with tightly controlled specifications on both silicon and quartz substrates<sup>25</sup>. The generic cross section of the CMUTs fabricated using this process is shown in Fig. 4. The highest process temperature of 250°C occurs during the PECVD of the silicon nitride layer which is used both as the isolation layer and the structural membrane layer. This temperature is low enough so that common metals such as aluminum and chromium can be used as the bottom electrode or as sacrificial layers. Furthermore, the substrate shown in Fig. 4 can be a silicon substrate with CMOS electronics with an oxide isolation layer enabling post-CMOS fabrication of CMUTs. The use of chromium as the sacrificial layer is advantageous since one can form very smooth films with 50nm thickness and perform sacrificial layer etching by commercial chrome etchant with high selectivity to silicon nitride. Figure 5-A shows the micrograph of CMUT IVUS array elements 6 hours into the chromium sacrificial layer etch. The dark region beneath the middle two membranes is the remaining chromium. The same bright color of the already etched membranes shows that the nitride membranes have the same thickness, i.e. they are not affected by the chromium etch. The AFM

image in Fig. 5-B shows a CMUT with a larger top electrode (80% of the membrane radius) which is designed as a result of coupling coefficient optimization models <sup>38,39</sup>.

Two critical capabilities of the CMUT fabrication process showing are depicted in Fig. 6. Figure 6-A shows a cross sectional scanning electron micrograph (SEM) of a 2 $\mu$ m diameter etch hole which is sealed by PECVD nitride. The 0.4 $\mu$ m thick top nitride layer used for electrode isolation and vacuum sealing can be distinctly seen, as well as the fact that the sealing occurs in the region only 0.5 $\mu$ m away from the etch hole edge. No long etch channels are needed for vacuum sealing and the CMUTs can be closely packed increasing the active area of the CMUT array element.



Figure 5. A) Micrograph of 2 IVUS array elements each consisting of  $1 \times 4$  32µm diameter circular membranes during sacrificial layer etch. B) 3-D AFM image of a similar CMUT membrane with larger electrode coverage

Furthermore, since the CMUT membrane is dielectric, one can embed more than one electrode in the membrane to form dual-electrode CMUTs for increased output power and receiver sensitivity. We have already fabricated and tested some of these devices. Figure 6-B shows the micrograph of a dual–electrode CMUT with  $20\mu m$  wide,  $300\mu m$  long silicon nitride membranes. Dielectric membranes deposited at low temperatures enable us to have multiple, electrically isolated electrodes buried in a single CMUT membrane. In this particular case two  $4\mu m$  wide side electrodes are connected to metal rail on the left and a separate center electrode is connected to the right. The doped silicon substrate serves as the ground plane. The design of dual-electrode CMUTs and some experimental results are discussed elsewhere<sup>25,40</sup>.



Fig. 6. A) SEM of a locally sealed etch hole. B) Top view of a dual-electrode CMUT.

#### 4. CHARACTERIZATION OF FORWARD-LOOKING CMUT-BASED IVUS ARRAYS

One of the advantages of CMUTs over piezoelectric transducers is the capability of building IVUS arrays with various shapes. An important array type is ring annular array which enables imaging totally occluded arteries, Doppler flow measurements and can guide interventions. We hav modeled, designed, and fabricated ring annular arrays for forward looking IVUS operating in the 10-25MHz range using the CMOS compatible low temperature process. Figure 7 shows the micrograph of a 64 element ring annular array built on silicon where each array element consists of 4 32µm diameter circular membranes (see Fig. 5-A). These arrays are suitable for imaging around 15MHz. We have also fabricated CMUT array elements with trapezoidal membranes with lateral dimensions in 40-45µm range for increased active area and operation in the lower frequency range (Fig. 7 inset, upper left corner). The number of array elements, and the overall array diameter of 0.9-1.2mm range are compatible with current solid-state IVUS systems and beamforming algorithms<sup>41</sup>. The exact geometrical dimensions, i.e. membrane thickness, gap thickness metallization area, of these devices have been determined using an electrical equivalent circuit and finite element analysis taking into account the DC bias requirements and the frequency of operation <sup>38</sup>.

These arrays have been electrically and acoustically characterized in detail. The arrays show excellent wafer to wafer uniformity in terms of mechanical resonance frequency and collapse voltage <sup>25</sup>. The pressure output and radiation pattern of these array elements were also measured to verify the transducer models and to find out about the problems such as acoustical cross talk. The pressure output of a single element in the array shown in Fig. 7 is measured using a hydrophone in a water tank. At a bias voltage of 60V (60% of collapse voltage in this case) the pressure output at the transducer surface is 20kPa/V and is constant over the 10-20MHz frequency range, which is in agreement with the model showing the broad bandwidth of the device.

Figures 8-A and 8-B show the measured radiation patterns of CMUT annular array elements (Fig. 7) when the array element is rotated around the short



Figure 7. Top view of a 64-element ring annular CMUT array for forward looking IVUS imaging. The inset shows part of another array with rectangular CMUT membranes.



Figure 8. A) Measured radiation pattern of a single element of the ring annular CMUT IVUS array shown in Fig. 7, when the array element is rotated around its short axis. B) The results of the same measurement when the array element is rotated around its long axis. The asymmetry in the measurement is due to the non-symmetrical epoxy distribution applied during packaging.

and long axis, respectively. The graphs shows the magnitude variation of the received signal with respect to rotation angle and frequency in MHz. The results are in good agreement with the diffraction model which predicts 6dB beamwidths of 100° and 50°, around the short and long axes at 15MHz, respectively. This patterns are suitable for forward looking IVUS arrays. The apparent bandwidth of the CMUT in these graphs is less than measured by pulse echo response measurements because the piezoelectric transducer used in the measurements has 40% bandwidth around 20MHz, limiting the measurement results. In addition to the side lobe information, these plots also show straight lines along the frequency axes around 17°, an indication of an interface wave on the silicon surface which can cause cross

talk problems. Detailed measurements on CMUTs built on silicon and quartz wafers show that these are due to surface waves in this frequency range<sup>22,24</sup>. Since the energy of these waves are predominantly trapped at the surface of the substrate, a thin polymer coating such parylene can be used to attenuate these propagation modes<sup>42</sup>.

The equivalent circuit model of the CMUT, which has been verified through impedance and pressure output measurements, suggests that these IVUS elements should provide 60dB/V dynamic range with 10MHz bandwidth assuming a low noise, low capacitance receiver amplifier. Therefore, with integrated electronics one can expect IVUS imaging with good resolution. To test the pulse-echo performance of these arrays on a medically relevant sample, a stent (Cypher<sup>®</sup> 3mm×18mm from Cordis) with approximately 100µm diameter stainless steel mesh is placed in front of a 1.2mm diameter 32 element ring annular CMUT array in a vegetable oil bath. The setup is shown in Fig. 9. Sixteen elements of the array are connected together and biased to 40V. While a negative voltage spike of 20V is applied to the transmitter, a single element is biased to 53V, close to the collapse voltage of 60V, and used as a receiver connected to a broadband amplifier (AD603).

Figure 10-A shows the measured pulse echo responses from the oilair interface, a 300µm diameter wire placed on a spacer, and the stent sample. The echo from the oil interface shows that there are some spurious pulses due to cross talk and possibly from the epoxy interfaces in the packaging. The echo signal from the wire is quite strong, indicating that attenuation in oil is effective at these frequencies. The echo signal from the front and back wires of the stent are clearly visible indicating a diameter of around 1.5mm. The frequency spectrum of the wire echo signal is shown in Fig. 10-B. As expected from the sharp pulses, the array elements show -10dB fractional bandwidth of 101% around 17.5MHz even with the notch due to surface wave crosstalk at 20MHz, and the large parasitic capacitance. As discussed above, the cross talk problems can be greatly reduced by thin polymer films deposited on the array surface, which would be the case in the packaging process of the IVUS catheters. Note that this bandwidth is a significant improvement over the existing phased array side looking IVUS arrays which have 20%



Figure 9. Experimental setup for the pulse echo test from a stent. The array and the stent are immersed in a 5mm deep oil bath in a Petri dish.



Figure 10. A) Pulse echo signals from different oil-air interface, a wire target, and a stent with  $100\mu$ m diameter stainless steel wire mesh. Multiple echoes in the stent indicate a diameter of about 1.5mm. B) The frequency spectrum of the main echo pulse from the wire target.

fractional bandwidth around 20MHz.

# 5. INITIAL IMAGING RESULTS WITH FORWARD-LOOKING CMUT-BASED IVUS ARRAYS

In order to demonstrate 3-D volumetric imaging with CMUT-based IVUS arrays, 16 channel receiver electronics has been built. Although the noise floor of this array electronics was quite high as compared to the single channel electronics due to shielding and electronic cross coupling problems on the cards, it has been possible to generate some initial results. The imaging data is obtained using a 32 element ring annular array, where 16 elements are connected in parallel as the transmitter. The schematic of the experiment is shown in Figure 11, where two 300µm diameter metal wires at different orientation and depth (3.7mm and 5.3mm) are used as targets. Again the CMUT array and targets are immersed in ~7mm deep vegetable oil. Pulse-echo signal obtained from one of the channels is also shown in Fig. 11. The signal to noise ratio (SNR) is not at the desired levels for real time imaging due to the high noise floor of the array electronics. Nevertheless, the different arrival times of the echoes from the two wires are clearly seen.

The data set is then processed offline using synthetic aperture reconstruction techniques to create 2-D slices of the 3-D volumetric image. Figure 12 shows two of these reconstructed slices on X=0 and Y=0 planes in linear scale. The echolucent background in the images contains speckle-like patterns due to poor SNR, and the streaks behind the wire targets are the result of the cross talk and ringing in the silicon substrate. Despite these artifacts the targets are clearly resolved and the side lobes are seen around the point-like targets on both slices. The asymmetric location and orientation of the targets with respect to origin is reflected by the difference in apparent target location as well as the orientation of the rings formed by the beamforming operations. These results show the feasibility of forward looking volumetric imaging with CMUT-based IVUS arrays.



Figure 11. Left: The schematic of the setup used for volumetric imaging experiments with annular CMUT IVUS imaging arrays. Right: The pulse echo signal obtained on one of the channels.

# 6. CONCLUSION

Capacitive micromachined ultrasonic transducer technology has become a viable alternative to piezoelectric transducers especially for ultrasonic imaging applications that require small array size and electronics integration. IVUS imaging is one of these applications. The CMUT fabrication process and the measured performance of the ring-annular CMUT arrays show that these 64-element CMUT arrays have the bandwidth and dynamic range required for forward looking IVUS in the 10-20MHz range. Further studies for CMOS electronics integration and IVUS catheter implementations seem to be natural next steps in the development of next generation CMUT based intravascular imaging devices.

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Figure 12. Left: One slice (on x = 0 plane) of the reconstructed volumetric image of the wire targets shown in Fig. 11. Right: Corresponding image on the y = 0 plane.

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